CPU Cards

CZGG LU-10-X

PISA Single-Board Computer with Embedded 1GHz CPU, VGA, SATA, IDE, Dual Gb LAN, CompactFlash Socket, USB & IrDA

RoHS compliant

USER'S MANUAL

VER. 1.2C • SEP 2007

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Title	CZGG LU-10-X	
Revision #	**Description**	**Date of Issue**
1.0	Initial Release	June 2006
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Glossary

AC '97	Audio Codec 97
ACPI	Advanced Configuration and Power Interface
APM	Advanced Power Management
ARMD	ATAPI Removable Media Device
ASKIR	Shift Keyed Infrared
ATA	Advanced Technology Attachments
BIOS	Basic Input/Output System
CFII	Compact Flash Type 2
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
Codec	Compressor/Decompressor
COM	Serial Port
DAC	Digital to Analog Converter
DDR	Double Data Rate
DIMM	Dual Inline Memory Module
DIO	Digital Input/Output
DMA	Direct Memory Access
EIDE	Enhanced IDE
EIST	Enhanced Intel SpeedStep Technology
FDD	Floppy Disk Drive
FDC	Floppy Disk Connector
FFIO	Flexible File Input/Output
FIFO	First In/First Out
FSB	Front Side Bus
IrDA	Infrared Data Association
HDD	Hard Disk Drive
IDE	Integrated Data Electronics
I/O	Input/Output
ICH4	I/O Controller Hub 4
L1 Cache	Level 1 Cache
L2 Cache	Level 2 Cache
LCD	Liquid Crystal Display
LPT	Parallel Port Connector
LVDS	Low Voltage Differential Signaling
MAC	Media Access Controller
OS	Operating System
PCI	Peripheral Connect Interface
PIO	Programmed Input Output
PnP	Plug and Play
POST	Power On Self Test
RAM	Random Access Memory
SATA	Serial ATA
S.M.A.R.T	Self Monitoring Analysis and Reporting Technology
SPD	Serial Presence Detect
S/PDI	Sony/Philips Digital Interface
SDRAM	Synchronous Dynamic Random Access Memory
SIR	Serial Infrared
UART	Universal Asynchronous Receiver-transmitter
USB	Universal Serial Bus
VGA	Video Graphics Adapter

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Chapter

1

Introduction

1.1 CZGG LU-10-X CPU Card Overview

The PISA form factor CZGG LU-10-X CPU card is fully equipped with a high performance, low power VIA processor and advanced multi-mode I/Os.

1.1.1 Models

The CZGG LU-10-X series has 1 CPU card model. See **Table 1-1**.

Model Name	Processor
CZGG LU-10-X	VIA LUKE 1GHz processor

Table 1-1: Model Variations

1.1.2 CZGG LU-10-X CPU Card Benefits

The CZGG LU-10-X is ideal for electronic devices that use flat panel displays including car entertainment systems, notebook computers and intelligent displays.

Some of the CZGG LU-10-X CPU card benefits include,

- providing access to multiple PCI and ISA expansion slots for easy system expansion
- operating reliably in harsh industrial environments with ambient temperatures as high as 60°C
- rebooting automatically if the BIOS watchdog timer detects that the system is no longer operating

1.1.3 CZGG LU-10-X CPU Card Features

Some of the CZGG LU-10-X CPU Card features are listed below:

- PISA half size CPU card
- RoHS compliant
- Low power, fanless processor
- Supports up to 1GB of 333MHz or 400MHz of DDR memory
- Dual high performance gigabit Ethernet (GbE) controllers onboard
- Eight USB 2.0 connectors
- One compact flash (CF) connector slot
- Two 150MB/s SATA drive channels
- Two gigabit Ethernet (GbE) channels
- One audio connector

- LVDS (optional), TTL and VGA monitor connectivity

1.2 CZGG LU-10-X CPU Card Connectors

1.2.1 CZGG LU-10-X Overview

The CZGG LU-10-X is a single board computer (SBC) that can be ordered with an ***optional*** LCDC LVDS-LUKE-A daughterboard, which provides improved LVDS connectivity. The LCDC LVDS-LUKE-A is mounted on the CPU Card, over the TTL connector. The connectors on both the LCDC LVDS-LUKE-A and the CZGG LU-10-X are introduced below. Unless specified at the time of order, the LCDC LVDS-LUKE-A is an optional accessory that will not arrive with your CZGG LU-10-X package; contact CyberResearch, Inc. for additional detail.

1.2.2 CZGG LU-10-X CPU Card Connectors

Figure 1-1 shows the connectors on the front side of the CZGG LU-10-X CPU card.

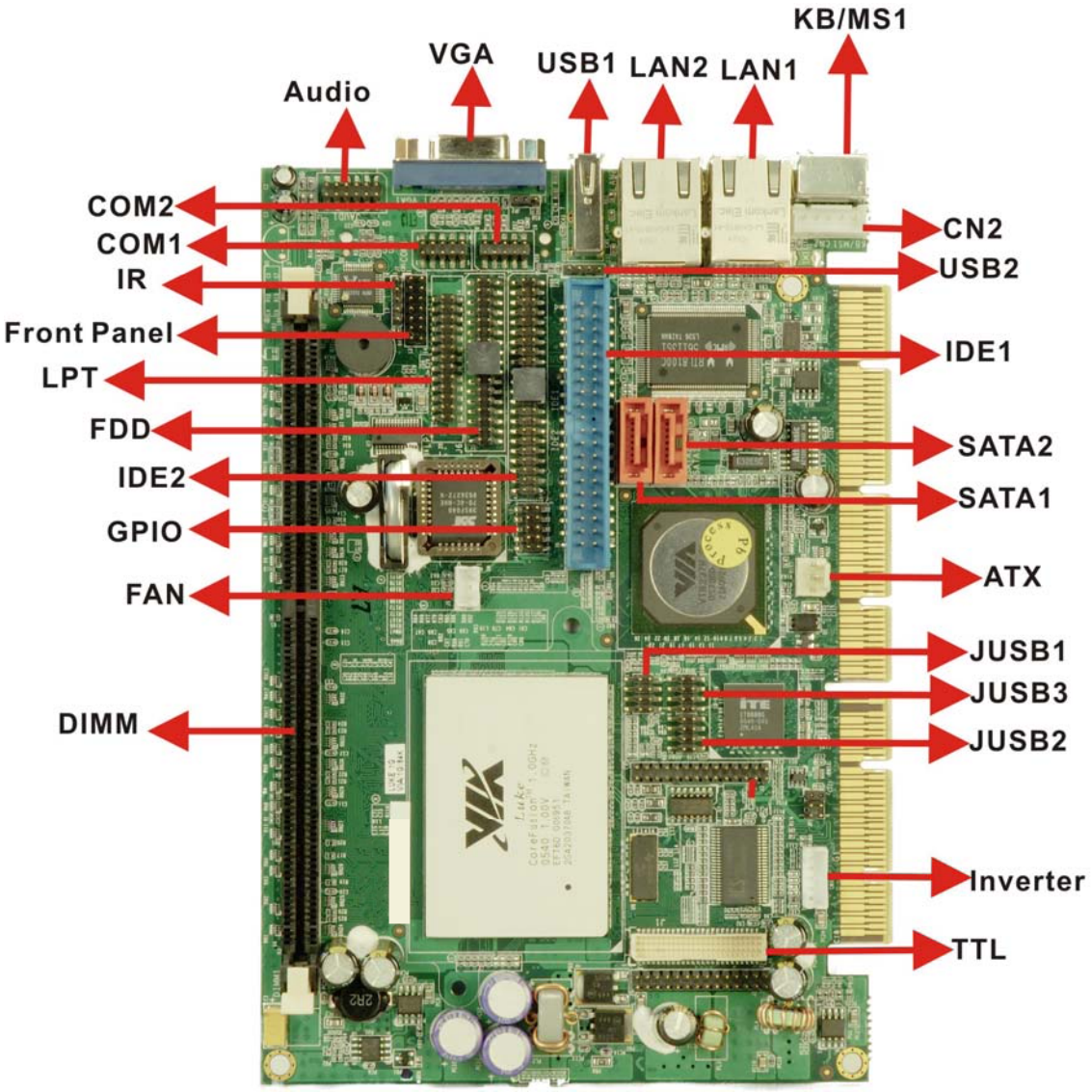

Figure 1-1: CZGG LU-10-X CPU Card Overview (Front Side)

The CZGG LU-10-X CPU card has the following connectors onboard and accessible on the front side of the CZGG LU-10-X (see **Figure 1-1**):

- 2 x IDE device connectors (primary and secondary)
- 1 x Floppy disk drive (FDD) connector
- 2 x SATA drive connectors
- 1 x Inverter connector
- 1 x TTL connector
- 1 x DIMM slot
- 1 x System fan connector
- 1 x GPIO connector

- 2 x RS-232C serial port connectors
- 1 x Infrared (IrDA) connector
- 3 x USB 2.0 connectors (each supports two devices)
- 1 x USB 2.0 connector (supports one device)
- 1 x USB 2.0 port
- 1 x Audio connector
- 1 x Parallel port connector
- 1 x Power supply to mainboard connector
- 1 x Front panel connector
- 1 x Keyboard/mouse connector

The CZGG LU-10-X CPU card also has the following jumpers accessible on the front side.

- Clear CMOS jumper
- LVDS voltage selection
- CF setup

Figure 1-2 shows the connectors on the reverse side of the CZGG LU-10-X CPU card.

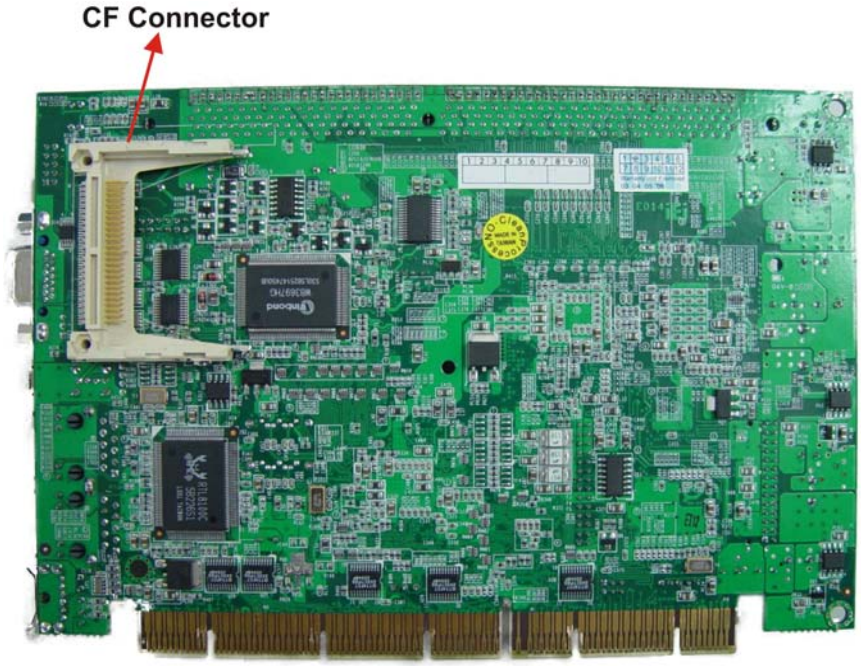

Figure 1-2: CZGG LU-10-X CPU Card Overview (Reverse Side)

The CZGG LU-10-X CPU card has the following connectors accessible on the reverse side of the CZGG LU-10-X (see **Figure 1-2**):

- 1 x Compact Flash II (CFII)

The CZGG LU-10-X CPU card has the following connectors on the board rear panel:

- 1 x PS/2

- 1 x VGA connector
- 2 x RJ-45 Ethernet connectors
- 1 x USB 2.0 ports

The location of these connectors on the CPU card can be seen in **Figure 1-1**. These connectors are fully described in **Chapter 3**.

1.2.3 (Optional) LCDC LVDS-LUKE-A Daughterboard Connectors

Figure 1-3 shows the connectors on the front side of the optional LCDC LVDS-LUKE-A expansion daughterboard.

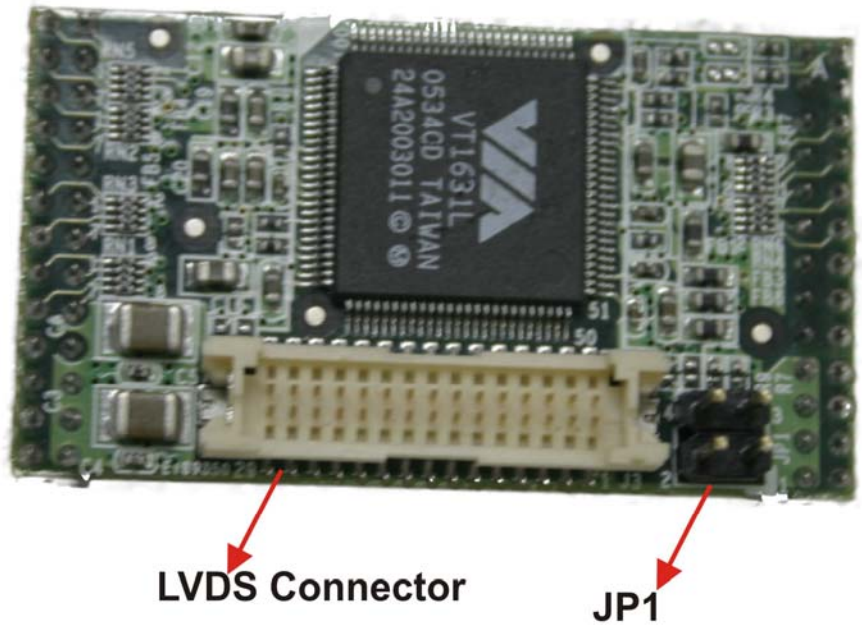

Figure 1-3: LCDC LVDS-LUKE-A Daughterboard Overview (Front Side)

The LCDC LVDS-LUKE-A has the following connectors onboard and accessible on the front side of the CZGG LU-10-X (see **Figure 1-3**):

- 1 x LVDS connector

The LCDC LVDS-LUKE-A has one jumper (JP1) accessible on the front side (see **Figure 1-3**). The jumper is used to set the voltage for the LVDS display.

1.3 Technical Specifications

1.3.1 CZGG LU-10-X CPU card Technical Specifications

CZGG LU-10-X CPU card technical specifications are listed in **Table 1-2**. Detailed descriptions of each specification can be found in **Chapter 2 Detailed Specifications**.

Specification	CZGG LU-10-X
Form Factor	PISA
CPU	1GHz VIA LUKE processor
System Chipset	VIA VT8237R+
Display	CRT
TTL	Dual 18-bit TTL LCD
Memory	Maximum Memory supported 1GB Support 333Mhz or 400MHz DDR 1x DDR DIMM socket supports up to 1GB
BIOS	AMI BIOS Label
Supper I/O	W83697HG
Audio	AC'97 2.3 Realtek ALC655
LAN	Dual RTL8100C for GbE
COM	2x RS232C
USB2.0	8x USB 2.0, 1 in rear, 7 by pin header
IDE	2x IDE connects to four devices
KB/MS	PS/2 connector and onboard pin header
WDT	Software programmable 1-255 sec. by supper I/O
IrDA	By super I/O
Digital I/O	4 input / 4 output by supper I/O
Fan connector	1x3 pin for CPU Fan
Power	AT/ATX support

Table 1-2: Technical Specifications

1.3.2 (Optional) LCDC LVDS-LUKE-A Daughterboard Technical Specifications

LCDC LVDS-LUKE-A technical specifications are listed in **Table 1-3**. Detailed descriptions of each specification can be found in **Chapter 2 Detailed Specifications**.

Specification	LCDC LVDS-LUKE-A
Chipset	VIA VT1631L
Display Connector	LVDS

Table 1-3: LCDC LVDS-LUKE-A Technical Specifications

Chapter

2

Detailed Specifications

2.1 Compatible CyberResearch Backplanes

The CZGG LU-10-X CPU card is compatible with all many CyberResearch, Inc. backplanes. For more information on these backplanes, please visit the www.cyberresearch.com or contact CyberResearch, Inc.

2.2 CPU Support

The CZGG LU-10-X CPU card comes with a preinstalled 1GHz, ultra low voltage (ULV) VIA® Luke processor. The new VIA 'Luke' CoreFusion Processing Platform integrates the latest generation VIA Eden-N™ processor with the VIA CN400 Northbridge in a single, low power package.

The Luke CoreFusion processor features include the following:

- **Rich Integration**:- *Highly integrated processing and digital media corelogic combination delivers leading performance in a single, power-efficient, space-saving package*
- **S3 Graphics Unichrome Pro Graphics Core**:- *With an internal data flow equivalent to what is available to the latest AGP 8X graphics cards, Unichrome Pro has separate 128-bit data path between the Northbridge for pixel data flow and texture/command access. Separate 128-bit 2D and 3D graphics engines ensure optimal performance for all multimedia, entertainment, and productivity applications.*
- **Flawless Digital Media Playback**:- *Unichrome Pro includes native support for the most popular digital video and audio playback through hardware MPEG-2/-4 acceleration and acclaimed VIA Vinyl Audio suite, delivering spectacular playback for entertainment devices.*
- **Maximum Display Flexibility**:- *Unichrome Pro with its optimized shared memory architecture and high definition video support through the Chromotion CE Video Display Engine, offers a breathtaking visual experience for the latest HDTV format displays. Support for LVDS and DVI interfaces enables complete flexibility for integration into a wide range of embedded and personal electronics applications*
- **Native Serial ATA**:- *The VIA DriveStaion™ Controller Suite with native dual channel Serial ATA controller provides direct support for two 150MB/s Serial ATA devices and the SATAlite™ interface expands support for two additional SATA devices.*

2.3 Southbridge Chipset

The CZGG LU-10-X CPU card has a VIA VT8237R Plus Southbridge on board. A summary of the available Southbridge features is listed below. For more information on this chipset please visit the VIA website.

- VIA DriveStation™ Controller Suite
  - Serial ATA
    - *Full duplex high performance 150MB/s Dual Channel Serial ATA interface*
    - *Support for additional two Serial ATA devices through SATALite™ interface*
  - Parallel ATA 133
    - *Supports up to four PATA devices*
- VIA Advanced Connectivity Suite
  - USB 2.0 Controller
  - Support for 8 USB 2.0/1.1 ports
    - *Network Controller*
  - Enterprise Class 10/100Mbps Fast Ethernet MAC
    - *PCI & LPC bus controllers*
- VIA Vinyl™ Audio
  - VIA Vinyl integrated 5.1 surround sound
    - *AC '97 audio*
    - *VIA Six-TRAC codec*
  - VIA Vinyl Gold onboard 7.1 surround sound
    - *24/96 resolution audio*
    - *VIA Envy24PT + VIA Six-TRAC Codec + additional DAC*
  - VIA Stylus Audio drivers
    - *Integrated Sensaura technology*
    - *Full 3D gaming support*
- V-MAP Architecture
  - Ultra V-Link
    - *High throughput 1GB/s South Bridge/North Bridge interconnect*
    - *Supports new generation VIA North Bridges across all processor platforms*
  - 8X V-Link
    - *High speed 533MB/s South Bridge/North Bridge interconnect*
    - *Supports current generation VIA North Bridges across all processor platforms*
  - VIA Hyperion 4in1 Unified Drivers
    - *Optimized system performance and stability*

2.4 Data Flow

Figure 2-1 shows the data flow between the two onboard chipsets and other components installed on the CPU card and described in the following sections of this chapter.

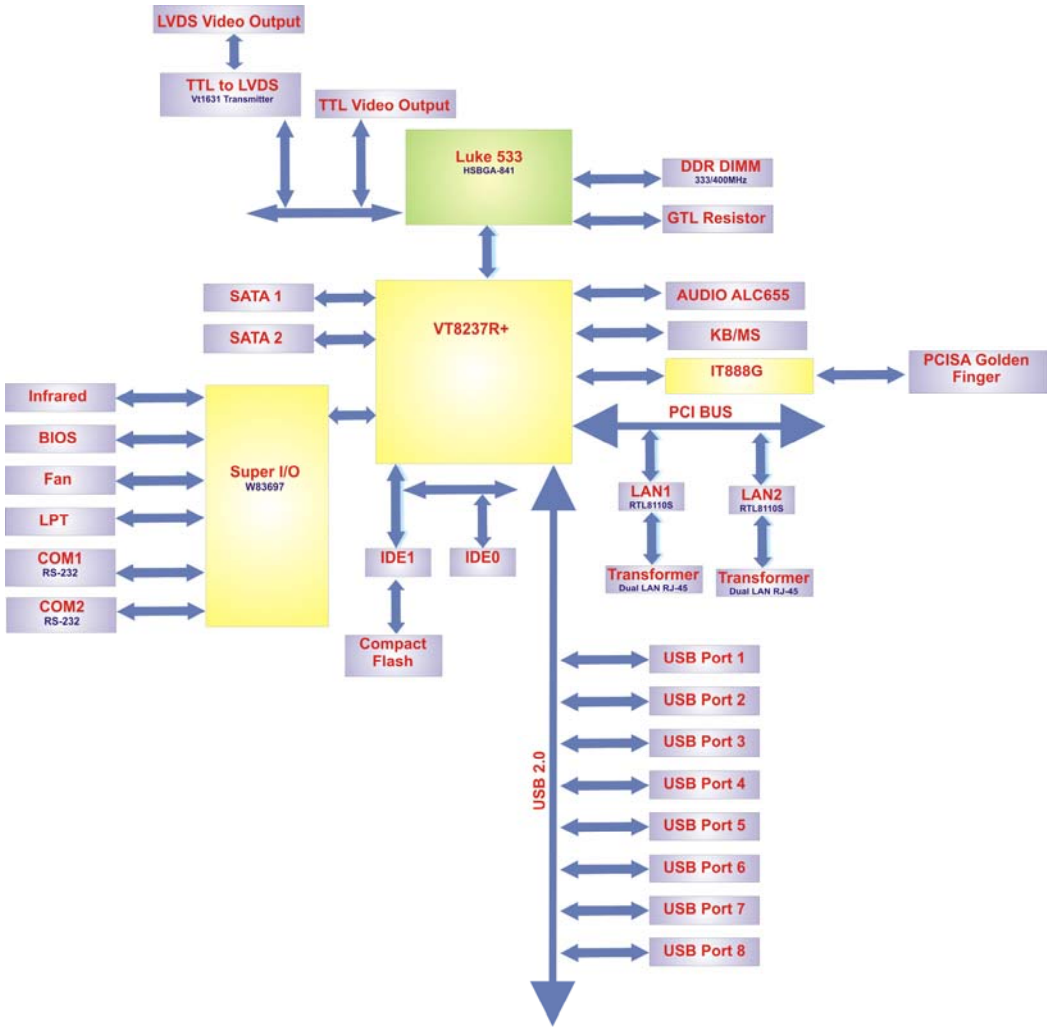

Figure 2-1: Data Flow Block Diagram

2.5

2.6 Graphics Support

The LUKE processor comes with a S3 Chromotion graphics engine. The features listed below are compatible with S3 Graphics' Chrome S20 Series processors:

- **Chromotion Video Acceleration**:-
  - **WMV9 Motion Compensation H/W Acceleration** – *Reduces CPU utilization when decoding Windows Media Video 9 (WMV9) files.*
  - **MPEG-2 IDCT and Motion Compensation H/W Acceleration** – *Reduces CPU utilization when decoding MPEG2 files.*
- **Chromotion Hi-Def™ Support**:-
  - **HDTV Formats** – *Supports all 18 DTV ATSC formats.*
  - **Adaptive Per-Pixel De-Interlacing** – *Produces superior image quality for both still and motion images using a high quality De-Interlacing process.*
  - **Video Deblocking** – *Removes blocking artifacts inherent in low bit rate images.*
  - **ChromoVision** – *Displays full screen video on secondary HDTV display while a windows display of the video is on the primary CRT or DVI display.*
  - **ChromoVision Modes with ChromeView Non-Linear Scaling** – *Scales a standard 4:3 image to fill a wide-screen 16:9 display with excellent image quality.*
  - **PanelDrive** – *Eliminates blurring effects with motion video on panel displays by increasing panel response time.*
  - **ChromoColor** – *Provides adjustment controls for the brightness, contrast, hue and saturation of the display of video.*
- **Chromotion Video Image Controls**:-
  - **ChromoColor Tonal Adjustment** – *Allows fine-tuning of luma values for the video display with controls for black point and white point enhancement.*
  - **ArtisticLicense Effects** – *Allows high quality image enhancements; including Sharpening, Soft Focus, Embossing, and Neon Edge effects.*

2.7 LVDS Display Support

The CZGG LU-10-X CPU card supports TTL displays. Using the ***optional*** LCDC LVDS-LUKE-A daughterboard enables connectivity to 18-bit or 24-bit flat panel displays. The LCDC LVDS-LUKE-A comes with an onboard VIA VT1631L Low Voltage Differential Signaling (LVDS) Transmitter. The VIA VT1631L is designed to support pixel data

transmissions from a Host to a Flat Panel display ranging from VGA to UXGA resolutions. Call or visit www.cyberresearch.com for more detail.

VIA VT1631 features are listed below.

- Complies with Open LDI Specification for Digital Display Interfaces
- 25 to 85 MHz Input Clock Support
- Supports VGA through UXGA Panel Resolution
- Power-down mode <198uW max (TBD)
- Two-wire Serial Communication Interface up to 400KHz
- Narrow Bus reduces cable size and cost
- Up to 4.76 Gbps bandwidth in dual 24-bit RGB into Dual Pixel Out applications
- Up to 592Mbytes/sec bandwidth
- Dual 12-bit double pumped digital input port
- PLL requires no external components
- Support both LVTTL and low voltage level input (Capable of 1.0 to 1.8V)
- Programmable input clock and control strobe select
- Compatible with TIA/EIA-644
- 2.24 to 2.75 supply voltage
- TQFP-100 Thin Quad Flat package

2.8 Memory Support

The CZGG LU-10-X CPU has one 184-pin dual inline memory module (DIMM) sockets and supports one 400MHz or 333MHz SDRAM DDR DIMM modules with a maximum RAM of up to 1GB.

2.9 PCI Bus Interface Support

The PCI bus on the CZGG LU-10-X CPU card has the following features:

- 33MHz Revision 2.2 is implemented
- Maximum throughput: 133MB/sec
- One PCI REQ/GNT pair can be given higher arbitration priority (intended for external 1394 host controller)
- 64-bit addressing supported

2.10 GbE Ethernet

The onboard Realtek RTL8100C is a highly integrated and cost-effective single-chip Fast Ethernet controller. It is enhanced with an ACPI (Advanced Configuration Power Interface) management function for PCI in order to provide efficient power management for

advanced operating systems with OSPM (Operating System Directed Power Management).

The onboard RTL8100C also supports remote wake-up to increase cost-efficiency in network maintenance and management.

Realtek RTL8100C Features

- 128-pin PQFP/LQFP (PQFP package pin-to-pin compatible with Realtek RTL8110S-32 Single-Chip Gigabit Ethernet Controller)
- Supports PCI/mini-PCI interfaces
- Integrates Fast Ethernet MAC, physical chip, and transceiver onto a single chip
- 10Mbps and 100Mbps operation
- Supports 10Mbps and 100Mbps N-way auto-negotiation
- Supports 25MHz Crystal or 25MHz OSC as the internal clock source
- Complies with PC99/PC2001 standards
- Supports ACPI power management
- Provides PCI bus master data transfer
- Provides PCI memory space or I/O space mapped data transfer
- Supports PCI clock speed of 16.75MHz-40MHz
- Advanced power saving mode
- Supports Wake-on-LAN and remote wake-up
- Half/Full duplex capability
- Supports Full Duplex Flow Control (IEEE 802.3x)
- Provides interface to 93C46 EEPROM to store resource configuration and ID parameters
- Provides PCI clock run pin
- Provides LED pins for network operation status indication
- 2.5/3.3V power supply with 5V tolerant I/Os
- 0.25µm CMOS process

2.11 Drive Interfaces

The CZGG LU-10-X can support the following drive interfaces.

- 2 x SATA drives
- 4 x IDE devices
- 1 x FDD
- 1 x Compact flash card

2.11.1 SATA Drive Support

The CZGG LU-10-X CPU card supports two, first generation SATA drives, with transfer rates up to 150MB/s.

2.11.2 IDE HDD Interfaces

The CZGG LU-10-X southbridge chipset IDE controller supports up to four HDDs with the following specifications:

- Supports PIO IDE transfers up to 16MB/s
- Supports Ultra ATA/133 devices with data transfer rates up to 133MB/s

2.11.3 Floppy Disk Drive (FDD)

The CZGG LU-10-X CPU card supports a single FDD. The following FDD formats are compatible with the board.

- 5.25": 360KB and 1.2MB
- 3.5": 720KB, 1.44MB and 2.88MB

2.11.4 Compact Flash Card

The CZGG LU-10-X CPU card supports standard CFII flash cards.

2.12 Serial Ports

The CZGG LU-10-X CPU card has two high-speed UART serial ports, configured as COM1 and COM2. The serial ports have the following specifications.

- 16C550 UART with 16-byte FIFO buffer
- 115.2Kbps transmission rate

2.13 Real Time Clock

256-byte battery backed CMOS RAM

2.14 System Monitoring

The CZGG LU-10-X CPU card is capable of self-monitoring various aspects of its operating status including:

- CPU, chipset, and battery voltage, +3.3V, +5V, and +12V
- RPM of cooling fans
- CPU and board temperatures (by the corresponding embedded sensors)

2.15 Infrared Data Association (IrDA) Interface

The CZGG LU-10-X CPU card IrDA supports the following interfaces.

- Serial Infrared (SIR)
- Shift Keyed Infrared (ASKIR)

If an IrDA port is used, the SIR or ASKIR mode must be configured in the BIOS under **Super IO devices**. The normal RS-232 COM 2 is then disabled.

2.16 USB Interfaces

The CZGG LU-10-X CPU card has eight USB interfaces, seven internal and one external. The USB interfaces support both USB 2.0 and USB 1.1.

2.17 BIOS

The CZGG LU-10-X CPU card uses a licensed copy of AMI BIOS. The features of the flash BIOS used are listed below:

- SMIBIOS (DMI) compliant
- Console redirection function support
- PXE (**P**re-Boot E**x**ecution **E**nvironment) support
- USB booting support

2.18 Operating Temperature and Temperature Control

The maximum and minimum operating temperatures for the CZGG LU-10-X CPU card are listed below.

- Minimum Operating Temperature: 0ºC (32°F)
- Maximum Operating Temperature: 60°C (140°F)

A heat sink must be installed on the CPU. Thermal paste must be smeared on the lower side of the heat sink before it is mounted on the CPU. Heat sinks are also mounted on the southbridge chipset to ensure the operating temperature of these chips remain low.

2.19 Audio Codec

The CZGG LU-10-X has an integrated REALTEK ALC655 codec. The ALC655 codec is a 16-bit, full-duplex AC'97 Rev. 2.3 compatible six-channel audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR-based designs. Some of the features of the codec are listed below.

- Meets performance requirements for audio on PC99/2001 systems
- Meets Microsoft WHQL/WLP 2.0 audio requirements
- 16-bit Stereo full-duplex CODEC with 48KHz sampling rate
- Compliant with AC'97 Rev 2.3 specifications

- Front-Out, Surround-Out, MIC-In and LINE-In Jack Sensing
- 14.318MHz -> 24.576MHz PLL to eliminate crystal
- 12.288MHz BITCLK input
- Integrated PCBEEP generator to save buzzer
- Interrupt capability
- Three analog line-level stereo inputs with 5-bit volume control, LINE_IN, CD, AUX
- High-quality differential CD input
- Two analog line-level mono inputs: PCBEEP, PHONE-IN
- Two software selectable MIC inputs
- Dedicated Front-MIC input for front panel applications (software selectable)
- Boost preamplifier for MIC input
- LINE input shared with surround output; MIC input shared with Center and LFE output
- Built-in 50mW/20ohm amplifier for both Front-out and Surround-Out
- External Amplifier Power Down (EAPD) capability
- Power management and enhanced power saving features
- Supports Power-Off CD function
- Adjustable VREFOUT control
- Supports 48KHz S/PDIF output, complying with AC'97 Rev 2.3 specifications
- Supports 32K/44.1K/48KHz S/PDIF input
- Power support: Digital: 3.3V; Analog: 3.3V/5V
- Standard 48-pin LQFP package
- EAX™ 1.0 & 2.0 compatible
- Direct Sound 3D™ compatible
- A3D™ compatible
- I3DL2 compatible
- HRTF 3D positional audio
- 10-band software equalizer
- Voice cancellation and key shifting in Karaoke mode
- AVRack® Media Player
- Configuration Panel for improved user convenience

2.20 Power Consumption

Table 2-1 shows the power consumption parameters for the CZGG LU-10-X CPU card when a 1GHz LUKE processor is running with one 256MB, 400MHz DDR module.

Voltage	Current
+5V	2A
+12V	0.073A

Table 2-1: Power Consumption

2.21 Packaged Contents

2.21.1 Package Contents

The following components are shipped with the CZGG LU-10-X.

- 1 x CZGG LU-10-X single board computer
- 1 x Mini jumper pack
- 1 x IDE flat cable 40p/40p/40p
- 2 x SATA cables
- 1 x SATA power cable
- 1 x RS-232 cable
- 1x USB cable
- 1 x Audio cable
- 1 x KB/PS2 Mouse Y cable
- 1 x Utility CD

2.21.2 Optional Accessory Items

The items shown in the list below are optional accessory items are purchased separately.

- LCDC LVDS-LUKE-A
- FDD cable
- LPT cable

Chapter

3

Connectors and Jumpers

3.1 Peripheral Interface Connectors

All peripheral interface connectors and jumpers on both the CZGG LU-10-X and LCDC LVDS-LUKE-A are shown in the sections below.

3.1.1 CZGG LU-10-X Peripheral Interface Connectors

Figure 3-1 and Figure 3-2 shows the onboard peripheral connectors, CPU card peripheral connectors and onboard jumpers.

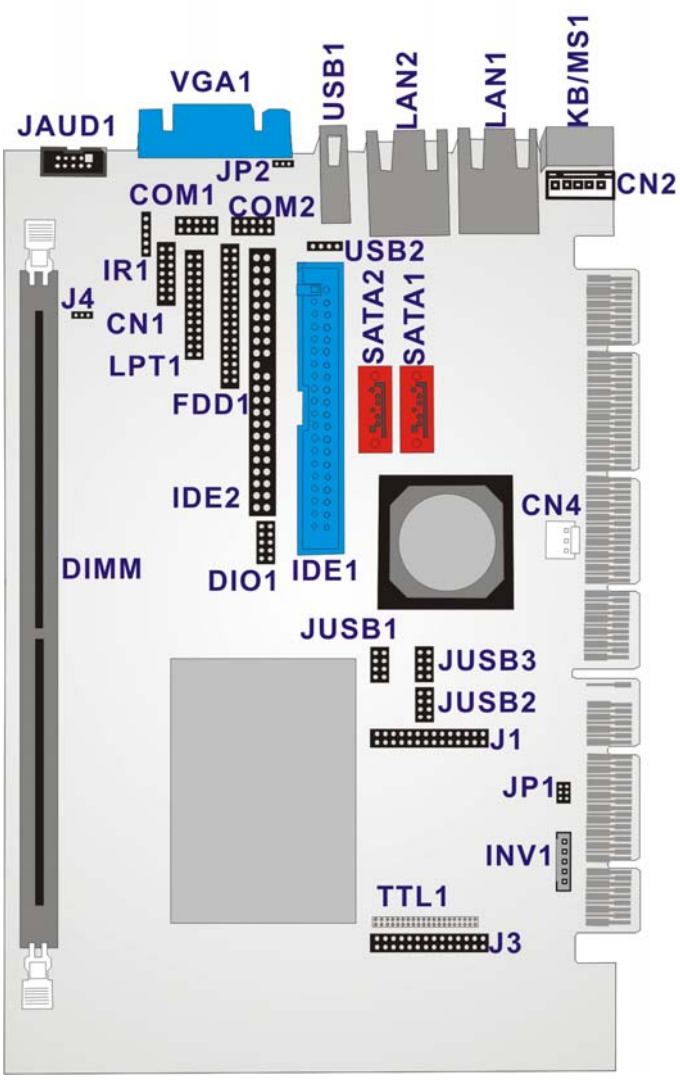

Figure 3-1: CZGG LU-10-X Connector and Jumper Locations (Front Side)

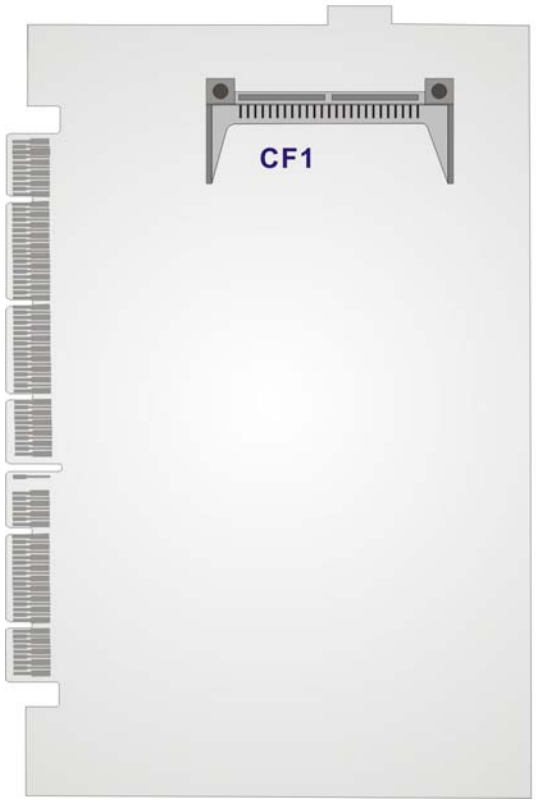

Figure 3-2: CZGG LU-10-X Connector Locations (Reverse Side)

Table 3-1 shows a list of the peripheral interface connectors on the CZGG LU-10-X CPU card Detailed descriptions of these connectors can be found in **Section 3.2** on **page 24**.

Connector	Type	Label
ATX PSON connector	**3-pin header**	**CN4**
Audio connector	**10-pin header**	**JAUD1**
Compact Flash (CF) connector	**50-pin header**	**CF1**
Fan connector	**3-pin header**	**FAN1**
Floppy Disk connector	**34-pin header**	**FDD1**
Front Panel connector	**12-pin header**	**CN1**
GPIO connector	**10-pin header**	**DIO1**
IDE Interface connector (Primary)	**40-pin header**	**IDE1**

IDE Interface connector (Secondary)	**44-pin header**	**IDE2**
Inverter Power connector	**5-pin header**	**INV1**
IR Interface connector	**5-pin header**	**IR1**
Keyboard connector	**5-pin header**	**CN2**
Parallel Port connector	**26-pin header**	**LPT1**
TTL connector	**40-pin header**	**TTL1**
USB connector (USB3 and USB4)	**8-pin header**	**JUSB1**
USB connector (USB5 and USB6)	**8-pin header**	**JUSB1**
USB connector (USB7 and USB8)	**8-pin header**	**JUSB1**

Table 3-1: Peripheral Interface Connectors

3.1.2 LCDC LVDS-LUKE-A Peripheral Interface Connectors

Figure 3-3 shows the onboard peripheral connector and onboard jumper of the LCDC LVDS-LUKE-A daughterboard.

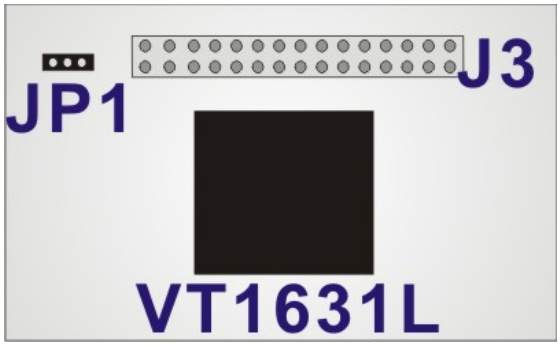

Figure 3-3: LCDC LVDS-LUKE-A Overview

3.1.3 Rear Panel Connectors

Figure 3-1 shows the rear panel connectors on the CZGG LU-10-X CPU card. Detailed descriptions of these connectors can be found in **Section 3.3**.

Connector	Type	Label
Ethernet connector	**RJ-45**	**LAN1**

Ethernet connector	**RJ-45**	**LAN2**
Keyboard/mouse connector	**PS/2**	**KB/MS1**
USB connector	**USB port**	**USB1**

Table 3-2: Rear Panel Connectors

3.1.4 Jumpers

Table 3-3 lists jumpers found on both the CZGG LU-10-X CPU card and the LCDC LVDS-LUKE-A. Detailed descriptions of these jumpers can be found in **Section 3.3.4** on **page 53**. (See **Figure 3-1** and **Figure 3-3** for jumper locations)

Description	Label	Type	Location
Clear CMOS	**J4**	**3-pin header**	**CZGG LU-10-X**
LCD voltage setup	**JP1**	**4-pin header**	**LCDC LVDS-LUKE-A**
CF card setup	**JP2**	**3-pin header**	**CZGG LU-10-X**

Table 3-3: Onboard Jumpers

3.2 Internal Peripheral Connectors

Internal peripheral connectors are found on the CPU card and are only accessible when the CPU card is outside of the chassis. This section has complete descriptions of all the internal, peripheral connectors on the CZGG LU-10-X CPU card and the LCDC LVDS-LUKE-A expansion daughterboard.

3.2.1 ATX PSON Connector

CN Label: **CN4**

CN Type: **3-pin header (1x3)**

CN Location: **See Figure 3-4**

CN Pinouts: **See Table 3-4**

The ATX PSON (CN4) connector connects to the backplane ATX connector. Refer to the backplane reference documents for more details.

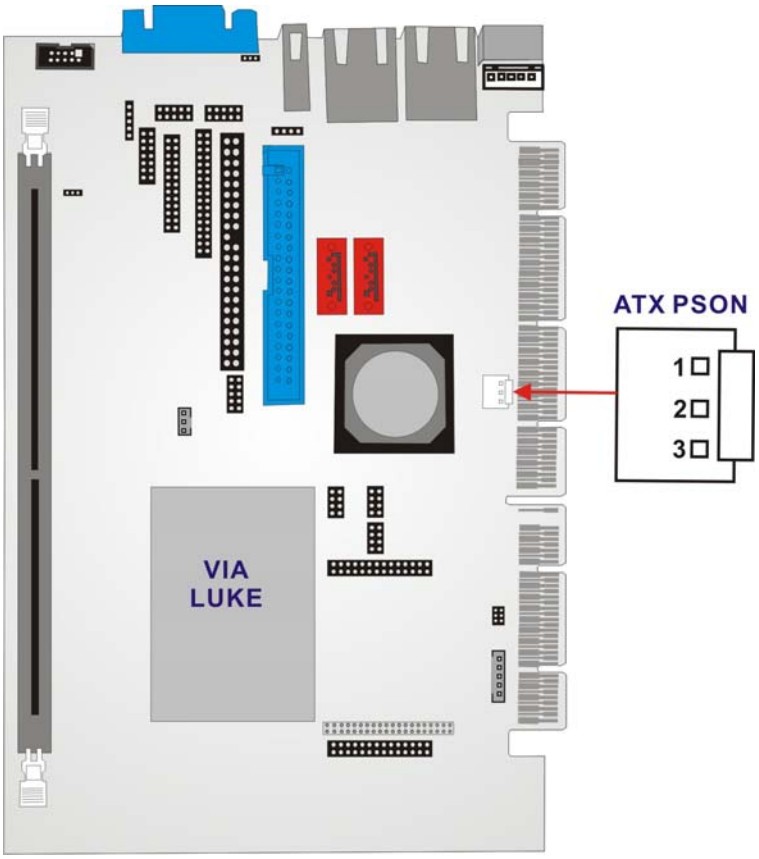

Figure 3-4: ATX PSON Pinouts

PIN NO.	DESCRIPTION
1	5V
2	PS_ON
3	GND

Table 3-4: ATX PSON Connector Pinouts

3.2.2 Audio Connector

CN Label: **JAUDIO1**

CN Type: **10-pin header (2x5)**

CN Location: **See Figure 3-5**

CN Pinouts: **See Table 3-5**

The onboard audio connector (JAUDIO1) is directly connected to an onboard AC'97 AUDIO CODEC. The audio connector directly connects to the MIC-IN, CD-IN and LINE-IN.

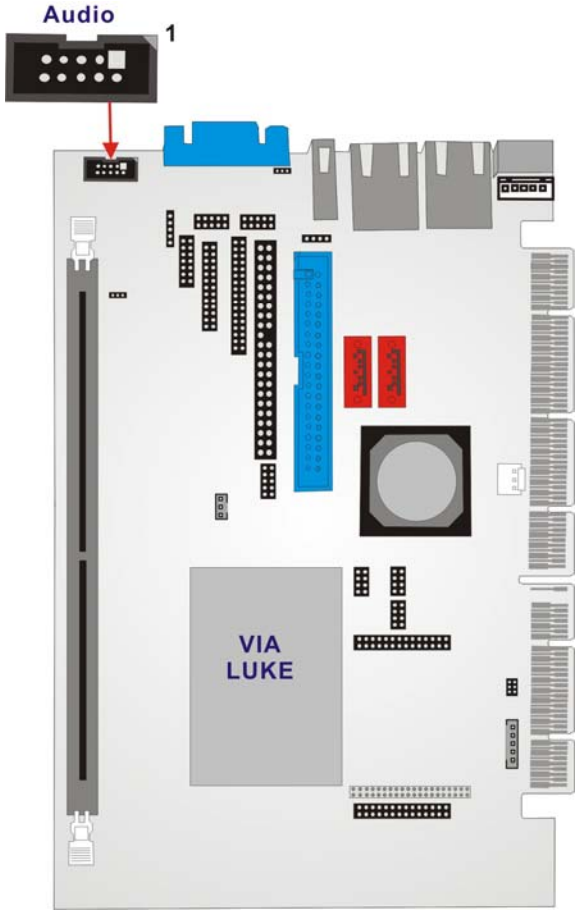

Figure 3-5: Audio Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	ROUT_L	2	LINR_L
3	GND	4	GND
5	LOUT_L	6	LINL_L
7	GND	8	GND
9	MICIN	10	

Table 3-5: Audio Connector Pinouts

3.2.3 Compact Flash Connector

CN Label: **CF1**

CN Type: **50-pin header (2x25)**

CN Location: **See Figure 3-6**

CN Pinouts: **See Table 3-6**

A compact flash memory module is inserted to the Compact Flash connector (CF1). Jumper 3 (JP3) configures the compact flash drive as either a slave or master device.

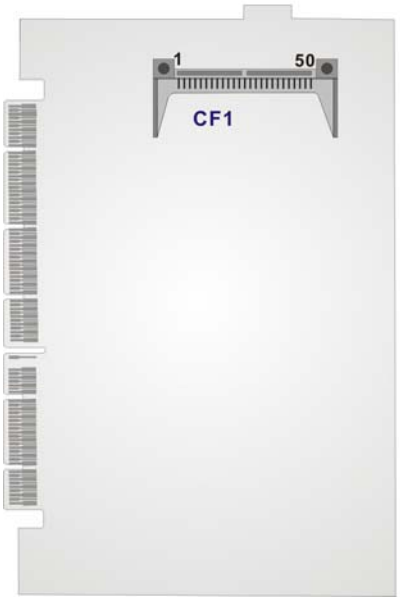

Figure 3-6: CF Flash Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GROUND	26	VCC-IN CHECK1
2	DATA 3	27	DATA 11
3	DATA 4	28	DATA 12
4	DATA 5	29	DATA 13
5	DATA 6	30	DATA 14
6	DATA 7	31	DATA 15
7	HDC_CS0#	32	HDC_CS1
8	N/C	33	N/C
9	GROUND	34	IOR#
10	N/C	35	IOW#
11	N/C	36	VCC_COM
12	N/C	37	IRQ15
13	VCC_COM	38	VCC_COM
14	N/C	39	CSEL
15	N/C	40	N/C
16	N/C	41	HDD_RESET
17	N/C	42	IORDY
18	SA2	43	SDREQ
19	SA1	44	SDACK#
20	SA0	45	HDD_ACTIVE#
21	DATA 0	46	66DET
22	DATA 1	47	DATA 8
23	DATA 2	48	DATA 9
24	N/C	49	DATA 10
25	VCC-IN CHECK2	50	GROUND

Table 3-6: Compact Flash Connector Pinouts

3.2.5 Fan Connector

CN Label: **FAN1**

CN Type: **3-pin header**

CN Location: **See Figure 3-7**

CN Pinouts: **See Table 3-7**

The cooling fan connector provides a 12V, 500mA current to a system cooling fan. The connector has a "rotation" pin to get rotation signals from fans and notify the system so the system BIOS can recognize the fan speed. Please note that only specified fans can issue the rotation signals.

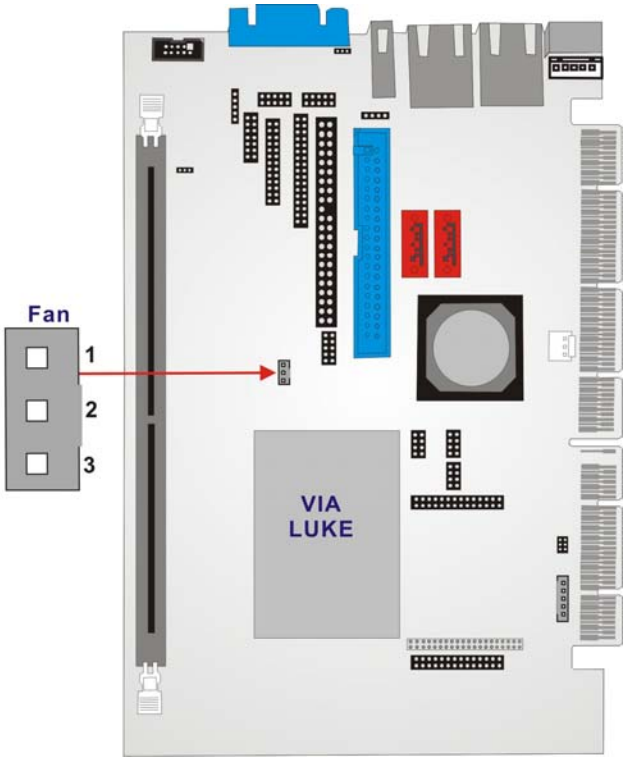

Figure 3-7: Fan Connector Pinout Locations

PIN NO.	DESCRIPTION
1	Fan Speed Detect
2	+5V
3	GND

Table 3-7: Fan Connector Pinouts

3.2.6 Floppy Disk Connector

CN Label: **FDD1**

CN Type: **34-pin header (2x17)**

CN Location: **See Figure 3-8**

CN Pinouts: **See Table 3-8**

The floppy disk connector (FDD1) is connected to a floppy disk drive.

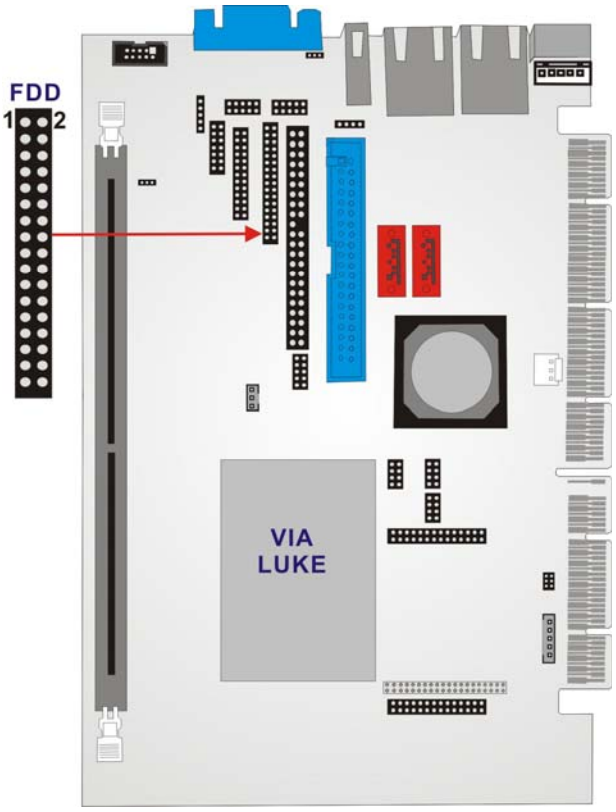

Figure 3-8: FDD Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	DRVDEN0
3	GND	4	N/C
5	GND	6	N/C
7	GND	8	-INDEX
9	GND	10	-MOA
11	GND	12	-DSB

13	GND	14	-DSA
15	GND	16	-MOB
17	GND	18	-DIR
19	GND	20	-STEP
21	GND	22	-WDATA
23	GND	24	-PWE
25	GND	26	-TRK0
27	N/C	28	-WPT
29	N/C	30	-RDATA
31	GND	32	-HDSEL
33	N/C	34	-DSKCHG

Table 3-8: Floppy Disk Connector Pinouts

3.2.7 Front Panel Connector

CN Label: **CN1**

CN Type: **14-pin header (2x7)**

CN Location: **See Figure 3-9**

CN Pinouts: **See Table 3-9**

The front panel connector (CN1) connects to several external switches and indicators to monitor and control the CPU card. These indicators and switches include:

- Power button
- Reset button
- Speaker
- Power LED
- HDD LED

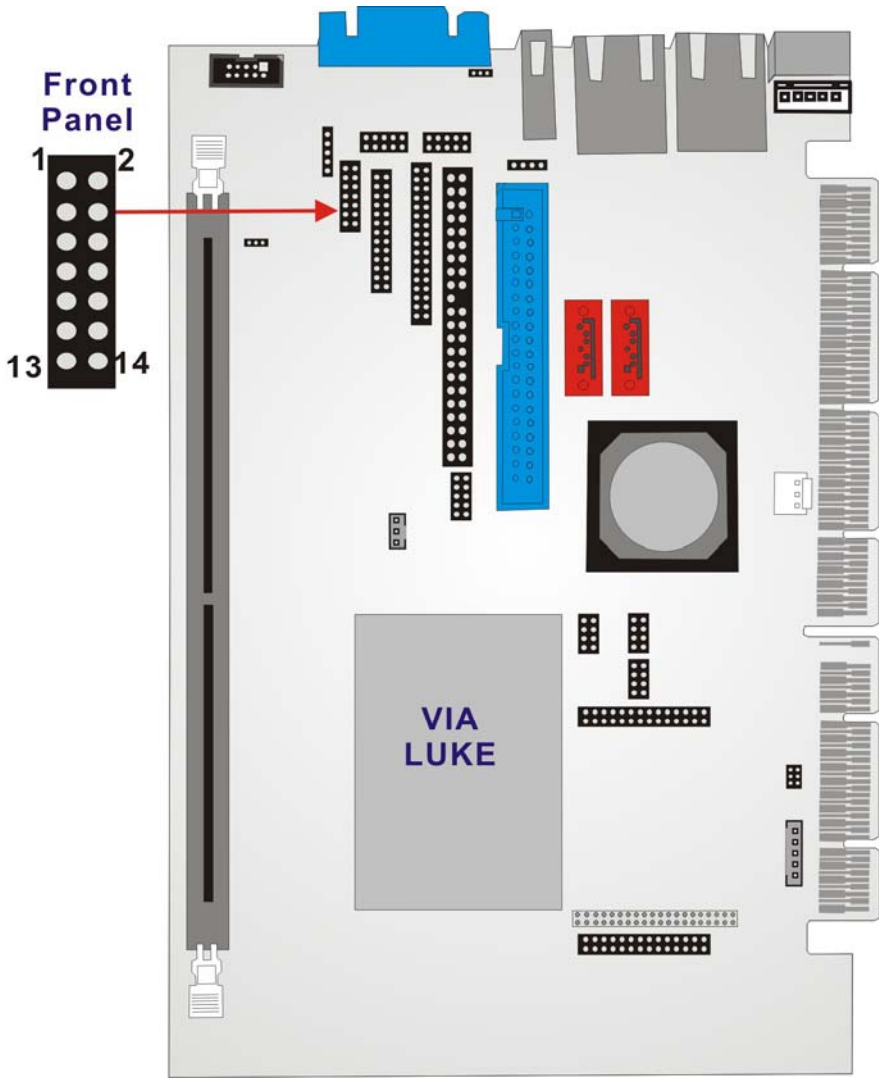

Figure 3-9: Front Panel Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1-5	POWER LED	2-8	SPEAKER
7-9	PWR BUTTON	12-14	RESET
11-13	HDLED		

Table 3-9: Front Panel Connector Pinouts

3.2.8 GPIO Connector

CN Label: **DIO1**

CN Type: **10-pin header (2x5)**

CN Location: **See Figure 3-10**

CN Pinouts: **See Table 3-10**

The General Purpose Input Output (GPIO) connector can be connected to external I/O control devices including sensors, lights, alarms and switches.

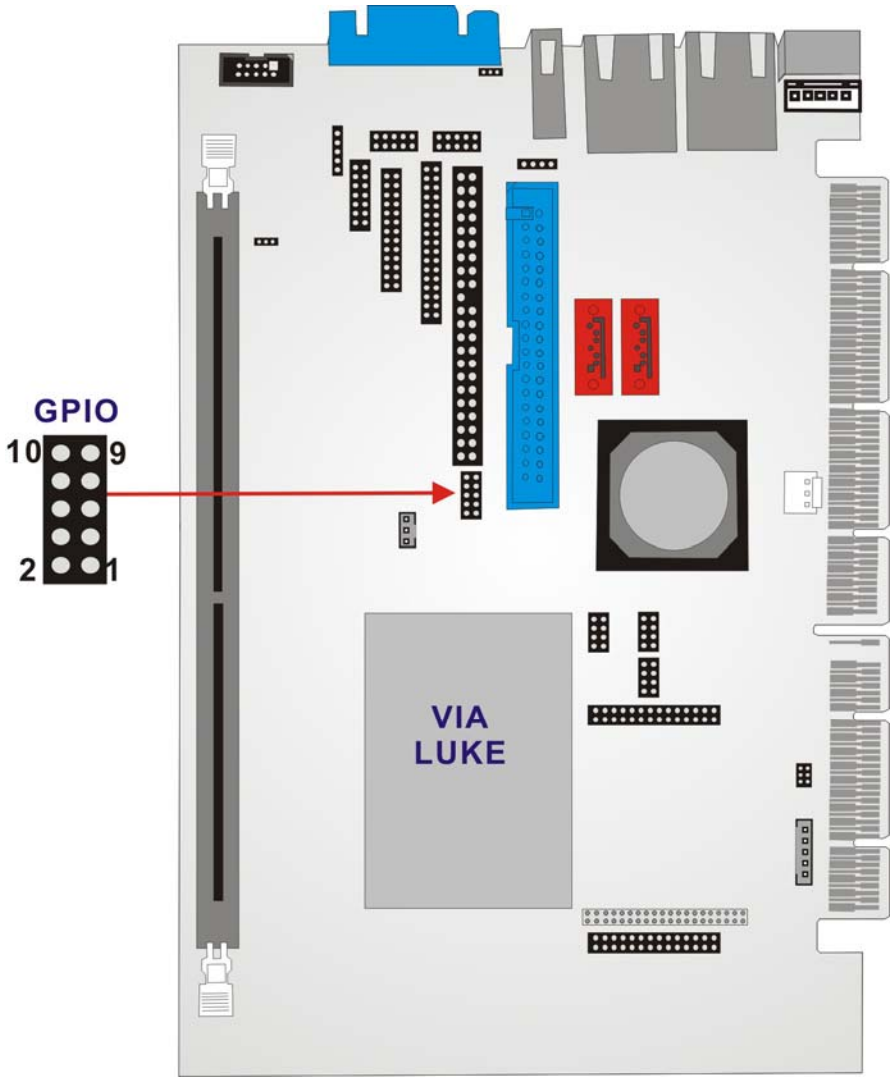

Figure 3-10: GPIO Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	5V
3	GP0	4	GP1
5	GP2	6	GP3
7	GP4	8	GP5
9	GP6	10	GP7

Table 3-10: GPIO Connector Pinouts

3.2.9 IDE Connector (Primary)

CN Label: **IDE1**

CN Type: **40-pin header (2x20)**

CN Location: **See Figure 3-11**

CN Pinouts: **See Table 3-11**

One primary 40-pin primary IDE device connector on the CZGG LU-10-X CPU card supports connectivity to Ultra ATA/133 IDE devices with data transfer rates up to 133MB/s.

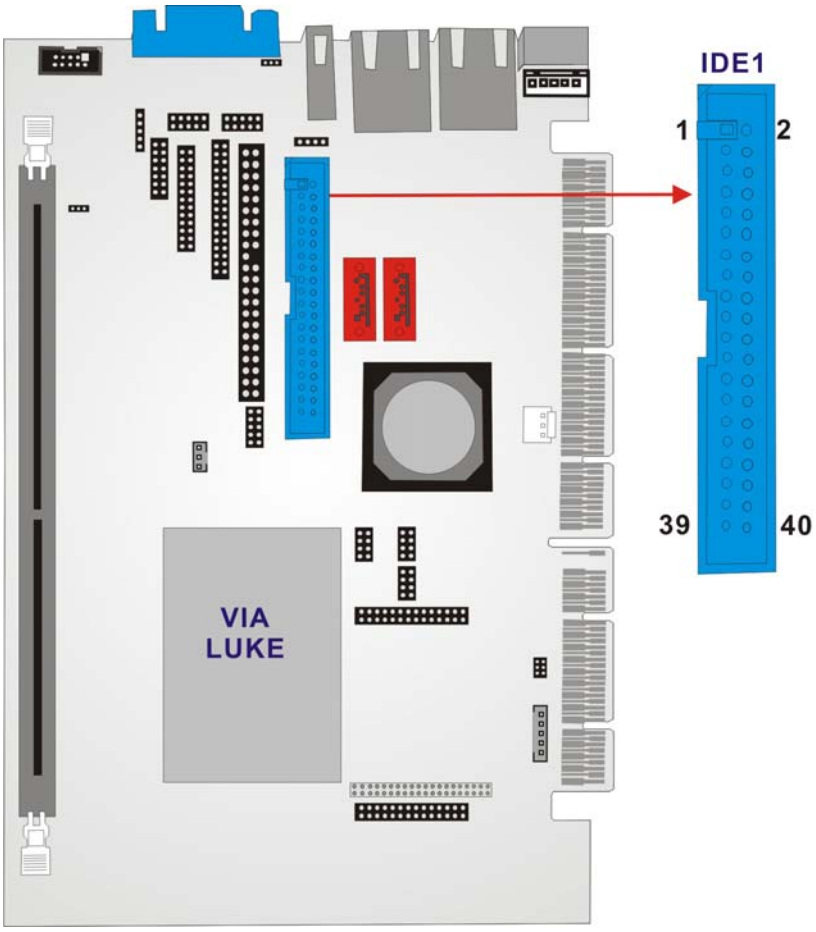

Figure 3-11: Primary IDE Device Connector Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	RESET#	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	N/C
21	IDE DRQ	22	GROUND

23	IOW#	24	GROUND
25	IOR#	26	GROUND
27	IDE CHRDY	28	GROUND
29	IDE DACK	30	GROUND–DEFAULT
31	INTERRUPT	32	N/C
33	SA1	34	N/C
35	SA0	36	SA2
37	HDC CS0#	38	HDC CS1#
39	HDD ACTIVE#	40	GROUND

Table 3-11: Primary IDE Connector Pinouts

3.2.10 IDE Connector (Secondary)

CN Label: **IDE2**

CN Type: **44pin header (2x22)**

CN Location: **See Figure 3-12**

CN Pinouts: **See Table 3-12**

One primary 44-pin secondary IDE device connector on the CZGG LU-10-X CPU card supports connectivity to Ultra ATA/133 IDE devices with data transfer rates up to 133MB/s.

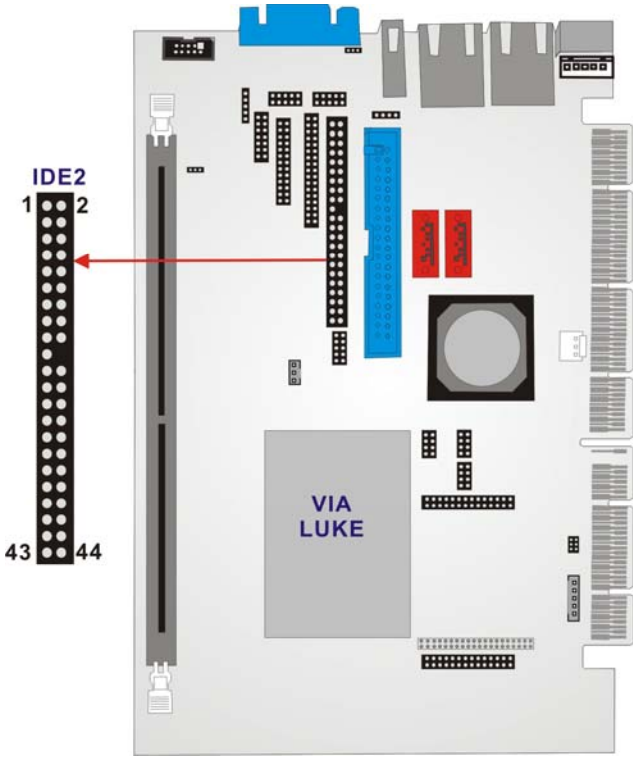

Figure 3-12: Secondary IDE Device Connector Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	RESET#	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	N/C
21	IDE DRQ	22	GROUND
23	IOW#	24	GROUND
25	IOR#	26	GROUND
27	IDE CHRDY	28	GROUND
29	IDE DACK	30	GROUND–DEFAULT

31	INTERRUPT	32	N/C
33	SA1	34	N/C
35	SA0	36	SA2
37	HDC CS0#	38	HDC CS1#
39	HDD ACTIVE#	40	GROUND
41	VCC	42	VCC
43	GROUND	44	N/C

Table 3-12: Secondary IDE Connector Pinouts

3.2.11 Inverter Power Connector

CN Label: **INV1**

CN Type: **5-pin header (1x5)**

CN Location: **See Figure 3-13**

CN Pinouts: **See Table 3-13**

The inverter connector is connected to the LCD backlight.

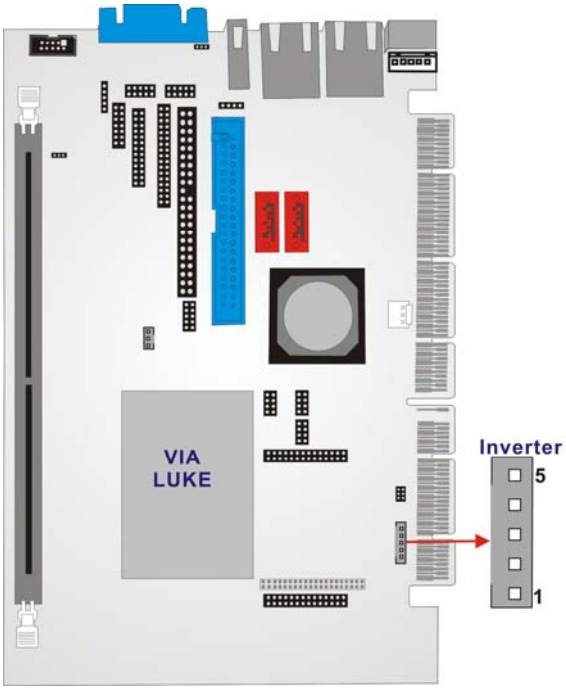

Figure 3-13: Inverter Connector Locations

PIN NO.	DESCRIPTION
1	NC
2	GND
3	12V
4	GND
5	EN_BL

Table 3-13: Inverter Power Connector Pinouts

3.2.12 IR Interface Connector

CN Label: **IR1**

CN Type: **5-pin header (1x5)**

CN Location: **See Figure 3-14**

CN Pinouts: **See Table 3-14**

The integrated infrared (IrDA) connector supports both Serial Infrared (SIR) and Amplitude Shift Key Infrared (ASKIR) interfaces.

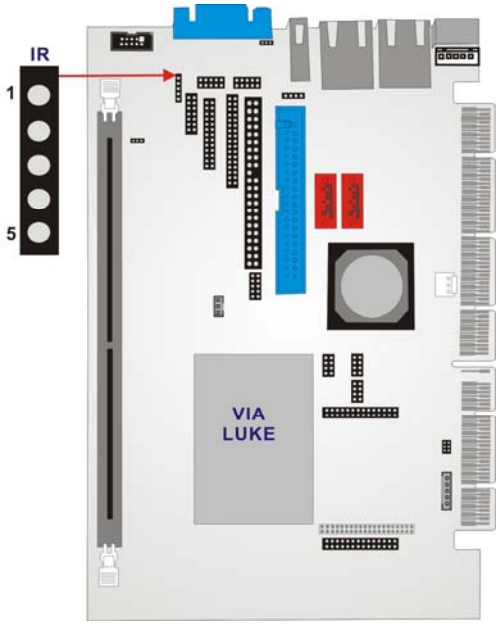

Figure 3-14: IR Connector Pinout Locations

PIN NO.	DESCRIPTION
1	5V
2	NC
3	IRRX
4	GND
5	IRTX

Table 3-14: IR Connector Pinouts

3.2.13 Keyboard Connector

CN Label: **CN2**

CN Type: **3-pin header (1x3)**

CN Location: **See Figure 3-15**

CN Pinouts: **See Table 3-15**

The keyboard connector (CN2 is connected to a keyboard if the PS/2 connector on the rear panel is connected to a mouse.

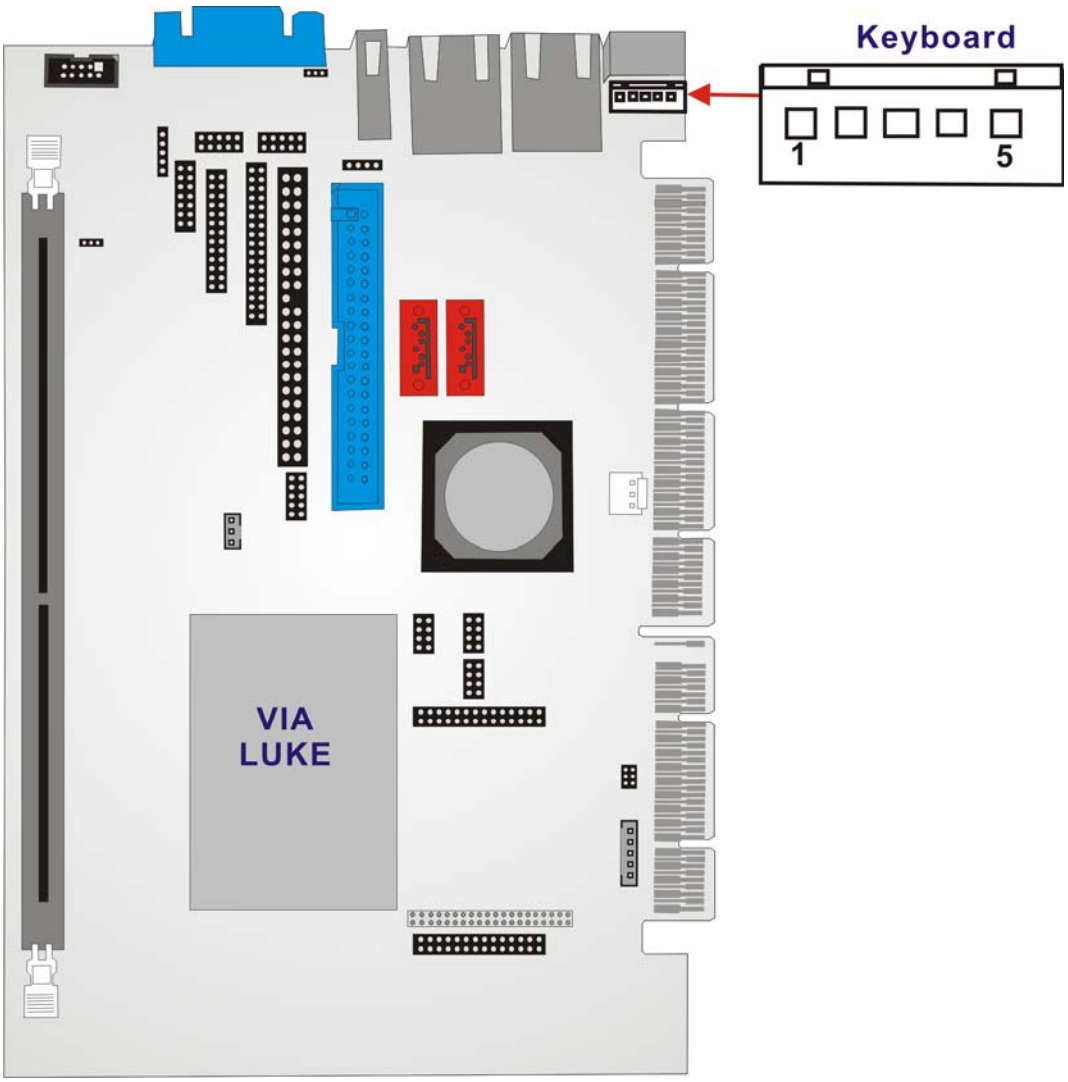

Figure 3-15: Keyboard Connector Pinout Locations

PIN NO.	DESCRIPTION
1	L_KCLK
2	L_KDAT
3	NC
4	GND
5	+5V

Table 3-15: Keyboard Connector Pinouts

3.2.14 LVDS Connector

CN Label: **J3 (on the *optional* LCDC LVDS-LUKE-A daughterboard)**

CN Type: **30-pin header (2x15)**

CN Location: **See Figure 3-15**

CN Pinouts: **See Table 3-15**

WARNING:

Make sure the daughterboard is correctly positioned on the CZGG LU-10-X CPU card connector pins. If the LCDC LVDS-LUKE-A is not correctly positioned irreparable damage to the CPU card, daughterboard and display may occur. Please refer to the installation instructions in ***Chapter 4***.

The LVDS LCD connector (J3) on the LCDC LVDS-LUKE-A daughterboard connects to a one or two channel (18-bit or 24-bit) LVDS panel.

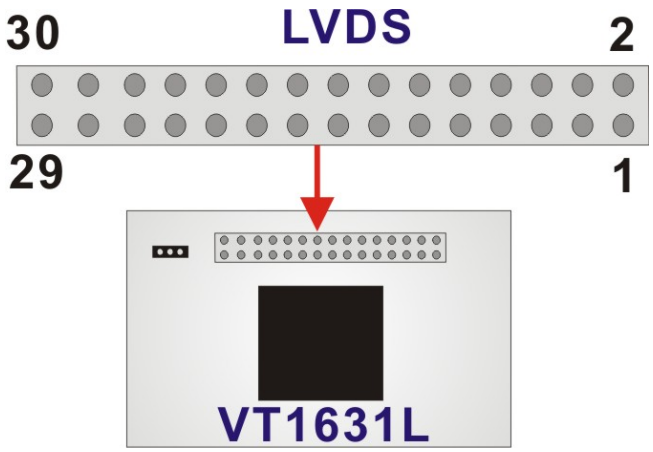

Figure 3-16: LVDS Connector Pinout Locations (on LCDC LVDS-LUKE-A)

PIN	DESCRIPTION	PIN	DESCRIPTION
1	GND	2	GND
3	1st LVDS data0 output +	4	1st LVDS data0 output -
5	1st LVDS data1 output +	6	1st LVDS data1 output -
7	1st LVDS data2 output +	8	1st LVDS data2 output -

9	1st LVDS clock output +	10	1st LVDS clock output -
11	1st LVDS data3 output +	12	1st LVDS data3 output -
13	GND	14	GND
15	2nd LVDS data0 output +	16	2nd LVDS data0 output -
17	2nd LVDS data1 output +	18	2nd LVDS data1 output -
19	2nd LVDS data2 output +	20	2nd LVDS data2 output -
21	2nd LVDS clock output +	22	2nd LVDS clock output -
23	2nd LVDS data3 output +	24	2nd LVDS data3 output -
25	GND	26	GND
27	+LCD (3.3V,5V or 12V)	28	+LCD (3.3V,5V or 12V)
29	+LCD (3.3V,5V or 12V)	30	+LCD (3.3V,5V or 12V)

Table 3-16: LVDS Connector Pinouts

3.2.15 Parallel Port Connector

CN Label: **LPT1**

CN Type: **26-pin header (2x13)**

CN Location: **See Figure 3-17**

CN Pinouts: **See Table 3-17**

The parallel port connector can be connected directly to parallel devices or to an external parallel port connector that is attached to the rear of a system chassis.

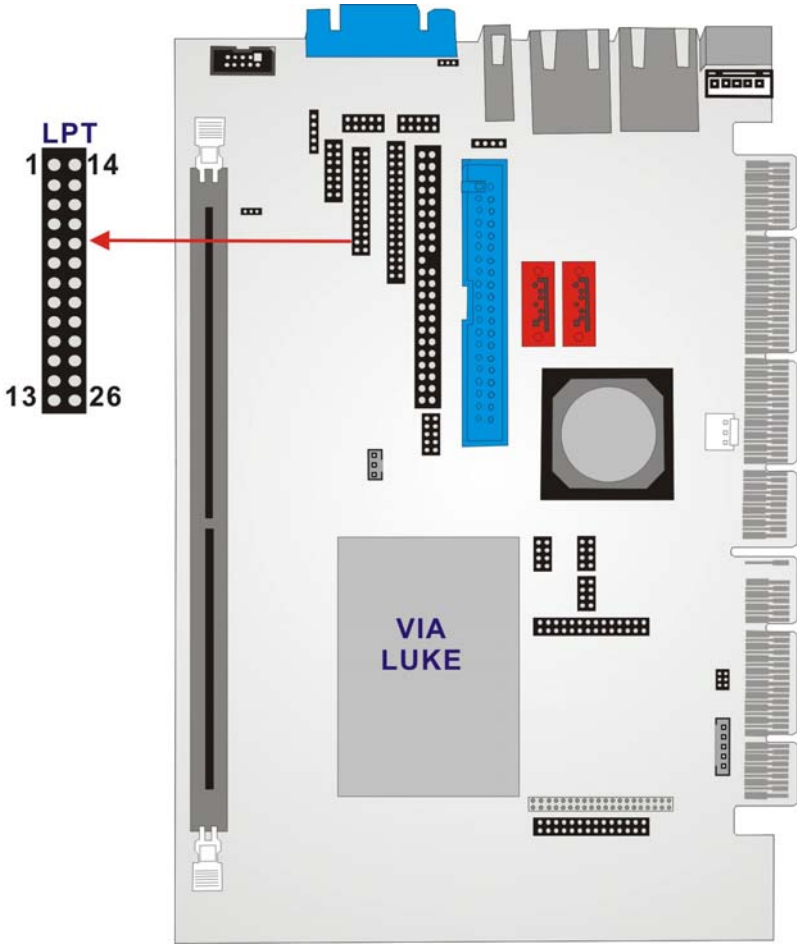

Figure 3-17: Parallel Port Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	STROBE#	2	DATA 0
3	DATA 1	4	DATA 2
5	DATA 3	6	DATA 4
7	DATA 5	8	DATA 6
9	DATA 7	10	ACKNOWLEDGE
11	BUSY	12	PAPER EMPTY
13	PRINTER SELECT	14	AUTO FORM FEED #
15	ERROR#	16	INITIALIZE
17	PRINTER SELECT LN#	18	GROUND
19	GROUND	20	GROUND
21	GROUND	22	GROUND

23	GROUND	24	N/C
25	GROUND	26	

Table 3-17: Parallel Port Connector Pinouts

3.2.16 SATA Connectors

CN Label: **COM1 and COM2**

CN Type: **2x5 pin header**

CN Location: **See Figure 3-18**

CN Pinouts: **See Table 3-18**

The Serial ATA (SATA) drive connectors are connected directly to 150MB/s SATA drives. The CZGG LU-10-X supports two SATA drives transmitting at speeds of up to 150MB/s.

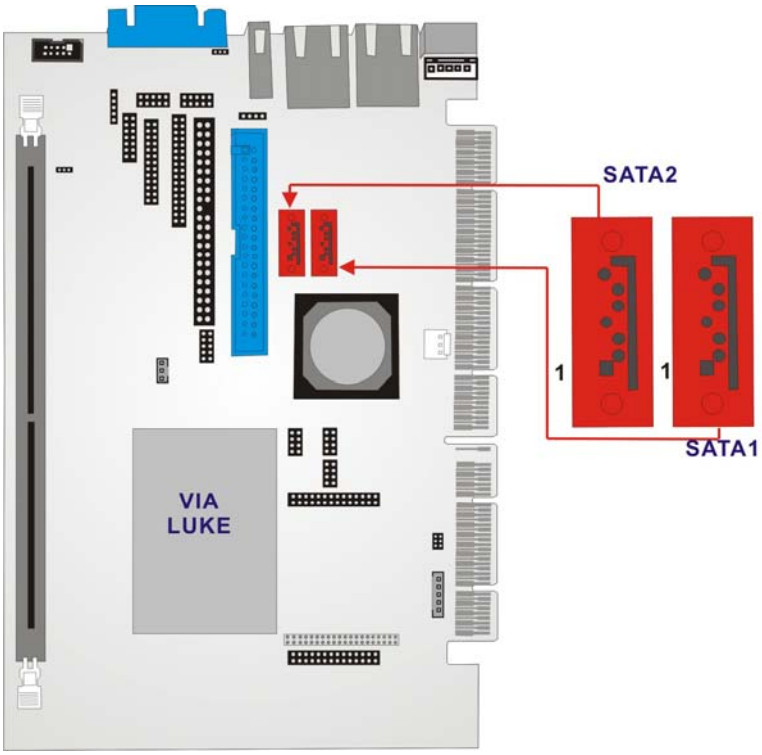

Figure 3-18: SATA Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	5	RX-
2	TX+	6	RX+
3	TX-	7	GND
4	GND		

Table 3-18: SATA Connector Pinouts

3.2.17 Serial Port Connectors

CN Label: **COM1 and COM2**

CN Type: **2x5 pin header**

CN Location: **See Figure 3-19**

CN Pinouts: **See Table 3-19**

The serial port connectors are used to connect to serial port devices. The two serial ports described here are both RS-232 compliant serial ports.

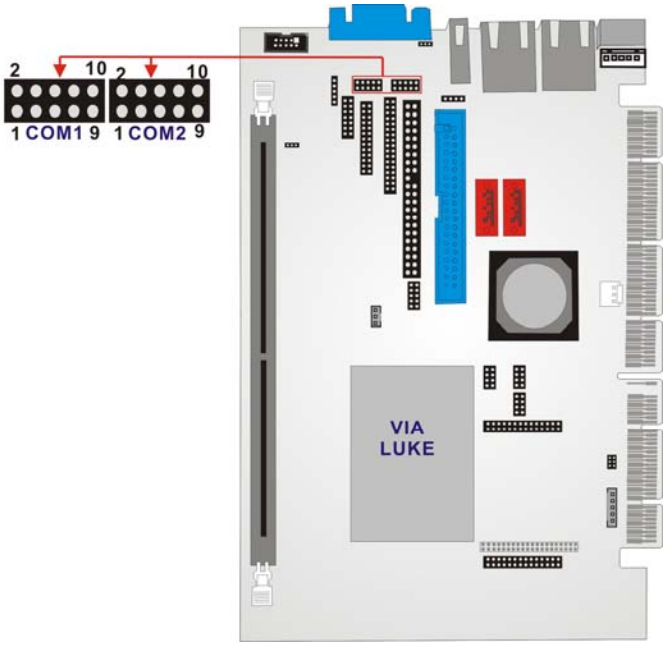

Figure 3-19: Serial Port Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	NDCD	2	NDSR
3	NRX	4	NRTS
5	NTX	6	NCTS
7	NDTR	8	NRI
9	GND	10	N/C

Table 3-19: Serial Port Connector Pinouts

3.2.18 TTL Interface Connector

CN Label: **TTL1**

CN Type: **40-pin header (2x20)**

CN Location: **See**

CN Pinouts: **See Table 3-20**

The TTL (tran

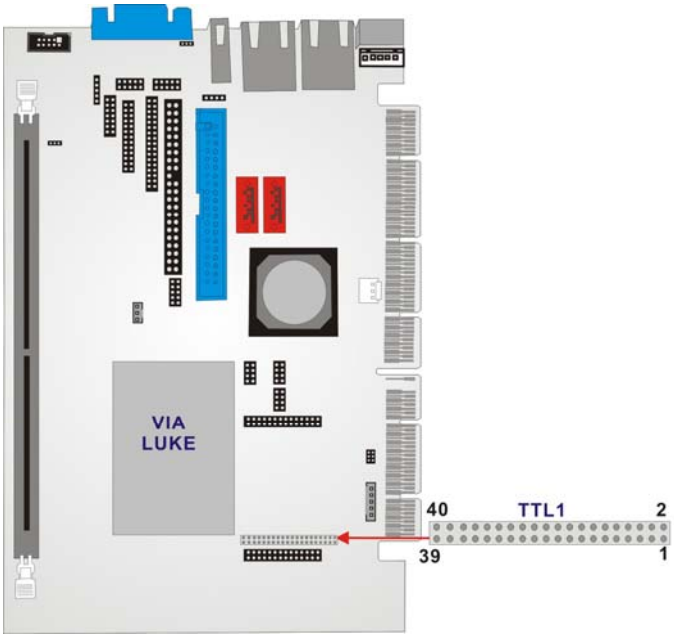

Figure 3-20: TTL Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
2	+LCD	1	+LCD
4	GND	3	GND
6	+LCD	5	N/C
8	GND	7	DATA 10
10	FPP1	9	FPP2
12	FPP3	11	FPP4
14	FPP5	13	FPP6
16	FPP7	15	FPP8
18	FPP9	17	FPP10
20	FPP11	19	FPP12
22	FPP13	21	FPP14
24	FPP15	23	FPP16
26	FPP17	25	FPP18
28	FPP19	27	FPP20
30	FPP21	29	FPP22
32	FPP23	31	FPP24
34	GND	33	GND
36	FPPVS	35	FPPCLKP
38	FPPHS	37	FPPDEN
40	ENPPVEE	39	N/C

Table 3-20: TTL Connector Pinouts

3.2.19 USB Connectors (Internal)

CN Label: **JSUB1, JSUB2, JSUB3**

CN Type: **8-pin header (2x4)**

CN Location: **See Figure 3-21**

CN Pinouts: **See Table 3-21 (USB2), Table 3-22 (JSUB1), Table 3-23 (JSUB2), Table 3-24 (JSUB3)**

One 4-pin (1x4) and three 8-pin (2x4) USB onboard connectors support seven USB 2.0 devices. Each USB connectors supports two USB2.0 devices.

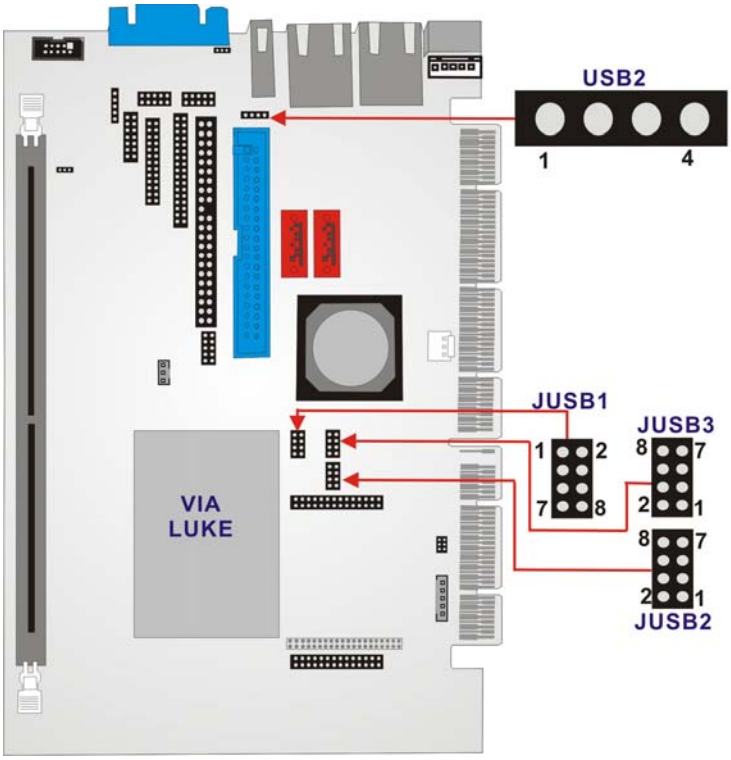

Figure 3-21: USBConnector Pinout Locations

PIN NO.	DESCRIPTION
1	+5V
3	USB_DT1-
5	USB_DT1+
7	GND

Table 3-21: USB2 Connector Pinouts

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	+5V	2	GND
3	USB_DT2-	4	USB_DT3+
5	USB_DT2+	6	USB_DT3-
7	GND	8	+5V

Table 3-22: JUSB1 Connector Pinouts

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	+5V	2	GND

3	USB_DT4-	4	USB_DT5+
5	USB_DT4+	6	USB_DT5-
7	GND	8	+5V

Table 3-23: JUSB2 Connector Pinouts

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	+5V	2	GND
3	USB_DT6-	4	USB_DT7+
5	USB_DT6+	6	USB_DT7-
7	GND	8	+5V

Table 3-24: JUSB3 Connector Pinouts

3.3 External (Rear Panel) Connectors

Figure 3-22 shows the CZGG LU-10-X CPU card rear panel. The peripheral connectors on the back panel can be connected to devices externally when the CPU card is installed in a chassis. The peripheral connectors on the rear panel are:

- 1 x PS/2 keyboard or mouse connector
- 2 x RJ-45 GbE connectors
- 1 x USB 2.0 connectors
- 1 x VGA connector

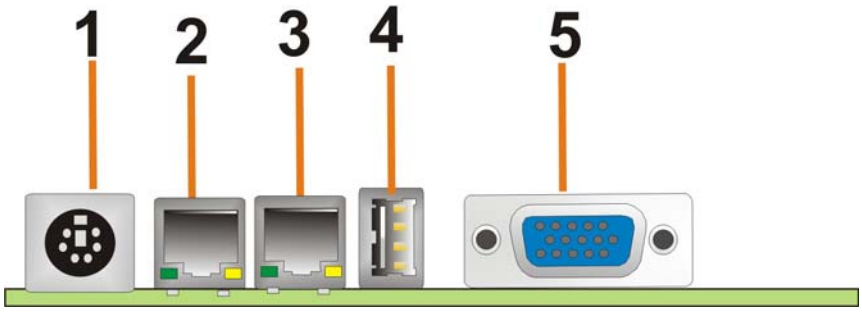

Figure 3-22: CZGG LU-10-X CPU card Rear Panel

3.3.1 Keyboard/Mouse Connector

CN Label: **KB_MS**

CN Type: **PS/2**

CN Location: **See Figure 3-22 (labeled number 1)**

CN Pinouts: **See Figure 3-23 and Table 3-25**

The CZGG LU-10-X keyboard or mouse connector is a standard PS/2 connectors.

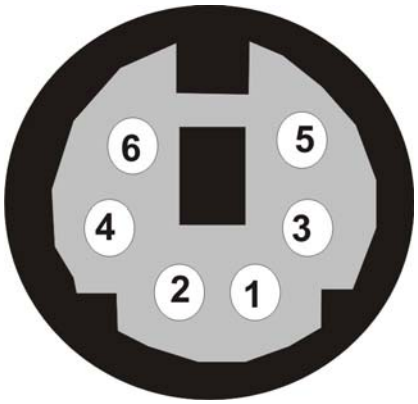

Figure 3-23: PS/2 Pinouts

PIN	DESCRIPTION	PIN	DESCRIPTION
1	KB_DATA	7	MS_DATA
2	NC	8	NC
3	GND	9	GND
4	+5V	10	+5V
5	KB_CLOCK	11	MS_CLOCK
6	NC	12	NC

Table 3-25: PS/2 Connector Pinouts

3.3.2 VGA connector

CN Label: **VGA1**

CN Type: **15-pin Female**

CN Location: **See Figure 3-22 (labeled number 5)**

CN Pinouts: **See Figure 3-24, Table 3-26 (VGA)**

The CZGG LU-10-X has a single 15-pin female connector for connectivity to standard display devices.

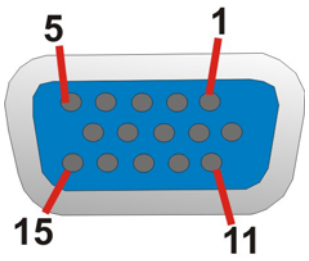

Figure 3-24: VGA Connector

PIN	DESCRIPTION	PIN	DESCRIPTION
1	RED	2	GREEN
3	BLUE	4	NC
5	GND	6	GND
7	GND	8	GND
9	VCC / NC	10	GND
11	NC	12	DDC DAT
13	HSYNC	14	VSYNC
15	DDCCLK		

Table 3-26: VGA Connector Pinouts

3.3.3 LAN Connectors

CN Label: **LAN1 and LAN2**

CN Type: **RJ-45**

CN Location: **See Figure 3-22 (labeled number 2 and 3)**

CN Pinouts: **See Table 3-27 (RJ-45)**

The CZGG LU-10-X is equipped with two built-in 10/100Mbps Ethernet controllers. The controllers connect to the LAN through two RJ-45 LAN connectors. There are two LED on the connector indicating the status of LAN. The pin assignments are listed in the following tables:

PIN	DESCRIPTION	PIN	DESCRIPTION
1	+2.5VCC	2	TX0+
3	TX0-	4	TX1+
5	TX1-	6	TX2+
7	TX2-	8	TX3+
9	TX3-	10	GND
11	LINK-	12	LINK+
13	ACTIVE-	14	ACTIVE+

Table 3-27: LAN Pinouts

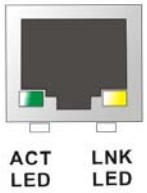

Figure 3-25: RJ-45 Ethernet Connector

The RJ-45 Ethernet connector has two status LEDs, one green and one yellow. The green LED indicates activity on the port and the yellow LED indicates the port is linked. See **Table 3-28**.

STATUS	DESCRIPTION	STATUS	DESCRIPTION
GREEN	Activity	YELLOW	Linked

Table 3-28: RJ-45 Ethernet Connector LEDs

3.3.4 USB Connector

CN Label: **USB1**

CN Type: **USB port**

CN Location: **See Figure 3-22 (LAN labeled number 4)**

The CZGG LU-10-X has a single USB 2.0 port accessible on the rear panel. This port is able to connect to both USB 2.0 and USB 1.1 devices. The pin assignments are listed in the following tables:

3.4 Onboard Jumpers

NOTE:

A jumper is a metal bridge that is used to close an electrical circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To CLOSE/SHORT a jumper means connecting the pins of the jumper with the plastic clip and to OPEN a jumper means removing the plastic clip from a jumper.

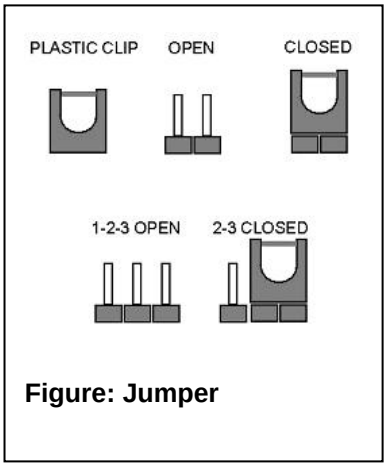

Figure: Jumper

The CZGG LU-10-X CPU card and daughter expansion board have nine onboard jumpers, two on the CPU card and six on the expansion daughterboard. The jumpers are described in **Table 3-29**.

Description	Label	Type	Location
Clear CMOS	**J4**	**3-pin header**	**CZGG LU-10-X**
LCD voltage setup	**JP1**	**6-pin header**	**CZGG LU-10-X**
CF card setup	**JP2**	**3-pin header**	**CZGG LU-10-X**
LVDS Setting	**JP3**	**4-pin header**	**LCDC** **LVDS-LUKE-A**

Table 3-29: Jumpers

3.4.1 LVDS Panel Voltage Selection Jumper

WARNING:

Making the wrong setting on this jumper may cause irreparable damage to both the CPU card and the LCD screen connected to the onboard connector.

Jumper Label: **JP1**

Jumper Type: **6 pin header**

Jumper Settings: **See Table 3-30**

Jumper Location: **See Figure 3-26**

This jumper allows the user to set the voltage for the LCD panel. Before setting this jumper please refer to the LCD panel user guide to determine the required voltage. After the required voltage is determined, make the necessary jumper setting in accordance with the settings shown in **Table 3-30**.

JP1	DESCRIPTION
Short 1-2	3V(Default)
Short 3-4	5V (Default)
Short 5-6	12V

Table 3-30: JP1 Jumper Settings

The pin locations are shown in Figure 3-26 below.

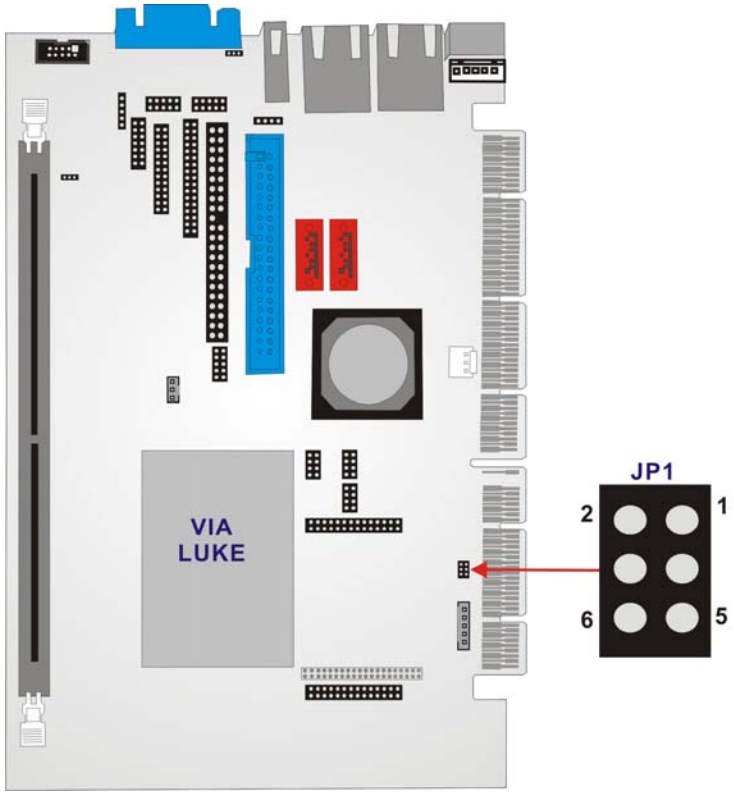

Figure 3-26: JP1 Pinout Locations

3.4.2 Reset CMOS Jumper

Jumper Label: **J4**

Jumper Type: **3 pin header**

Jumper Settings: **See Table 3-31**

Jumper Location: **See Figure 3-27**

If the CPU Card fails to boot due to improper BIOS setting, use this jumper to clear the CMOS data and reset the system BIOS information. To do this, use the jumper cap to close pins 2 and 3 for a few seconds then reinstall the jumper clip back to pins 1 and 2.

If the "CMOS Settings Wrong" message displays during the boot up process, the fault can be corrected by pressing the F1 to enter the CMOS Setup menu. Then do one of the following:

- Enter the correct CMOS setting
- Load Optimal Defaults
- Load Failsafe Defaults.

After the above is completed, save the changes and exit the CMOS Setup menu.

Clear CMOS	DESCRIPTION
1-2 (Default)	Keep CMOS Setup
2-3	Clear CMOS Setup

Table 3-31: Clear CMOS Jumper Settings

The clear CMOS jumper is located in Figure 3-27.

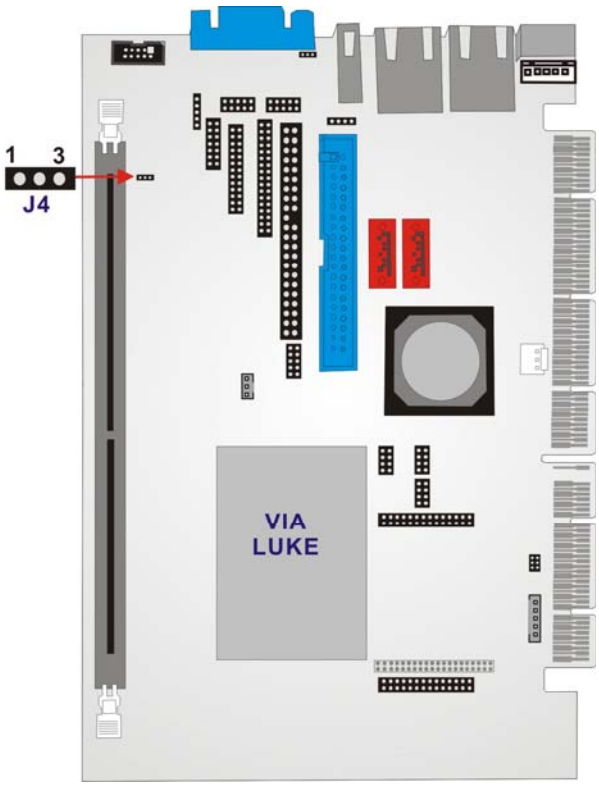

Figure 3-27: CLR_CMOS Pinout Locations

3.4.3 CF Card Setup

Jumper Label: **JP3**

Jumper Type: **3-pin header**

Jumper Settings: **See**

Jumper Location: **See Figure 3-28**

The JP3 jumper sets the compact flash card as either the slave device or the master device.

CF Card Setup	DESCRIPTION
Short 2-3	Slave(Default)
Short 1-2	Master

Table 3-32: CF Card Setup Jumper Settings

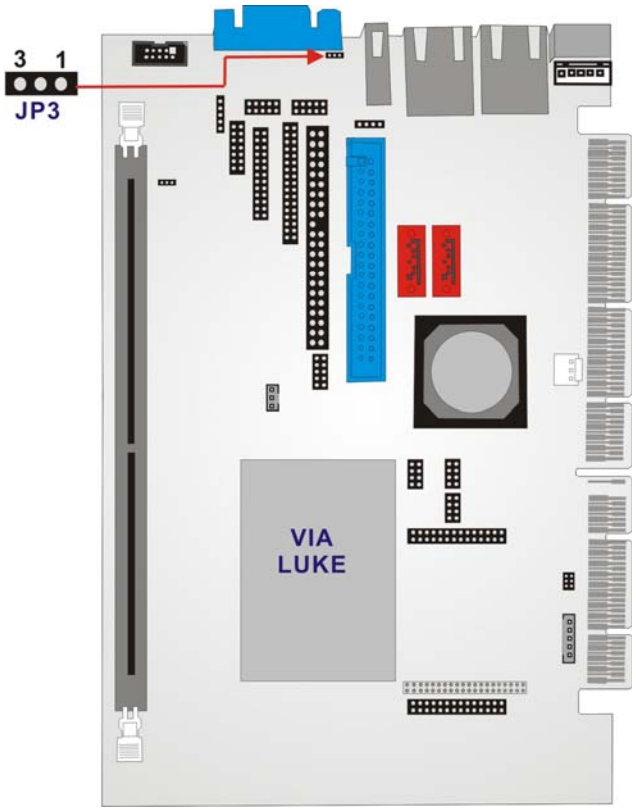

Figure 3-28: JP4 Pinout Locations

3.4.4 LVDS Voltage Selection

WARNING:

Making the wrong setting on this jumper may cause irreparable damage to both the CPU card and the LCD screen connected to the onboard connector.

Jumper Label: **JP1 (on the *optional* LCDC LVDS-LUKE-A)**

Jumper Type: **4-pin header**

Jumper Settings: **See**

Jumper Location: **See Figure 3-28**

This jumper configures the LVDS flat panel screen. The jumper settings are in the table below:

LVDS	DESCRIPTION
1-2	Open : Dual Channel (Default) Short : Single Channel
3-4	Open : Single-Ended Clock (Default) Short : Dual Clock

Table 3-33: LVDS Jumper Settings

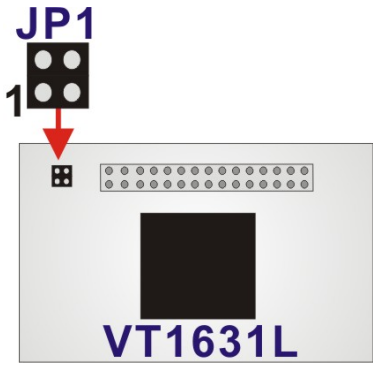

Figure 3-29: LVDS Jumper Pinout Locations

Chapter

4

Installation and Configuration

4.1 Installation Considerations

NOTE:

The following installation notices and installation considerations should be read and understood before the CPU card is installed. All installation notices pertaining to the installation of the CPU card should be strictly adhered to. Failing to adhere to these precautions may lead to severe damage of the CPU card and injury to the person installing the CPU card.

4.1.1 Installation Notices

Before and during the installation of the CZGG LU-10-X CPU card, please **do** the following:

- Read the user manual
  - The user manual provides a complete description of the CZGG LU-10-X CPU card, installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD)
  - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the user's body and help to prevent ESD damage.
- Place the CPU Card on an antistatic pad
  - When the CPU Card is installed and configured, place it on an antistatic pad. This helps to prevent potential ESD damage.
- Turn off all power to the CZGG LU-10-X CPU card
  - When working with the CPU card, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the CZGG LU-10-X CPU card, **DO NOT:**

- remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- use the product before all the cables and power connectors are properly connected.
- allow screws to come in contact with the PCB circuit, connector pins, or its components.

4.2 Unpacking

NOTE:

If any of the items listed below are missing when the CZGG LU-10-X is unpacked, do not proceed with the installation and contact CyberResearch, Inc. immediately.

4.2.1 Unpacking Precautions

Some components on CZGG LU-10-X are very sensitive to static electricity and can be damaged by a sudden rush of power. To protect it from being damaged during the unpacking process, follow these precautions:

- The user should be grounded to remove any static charge before touching the CZGG LU-10-X . Users can wear a grounded wrist strap at all times or frequently touch any conducting material that is connected to the ground to discharge static electricity.
- Handle the CZGG LU-10-X by its edges. Do not touch the IC chips, leads or circuitry unnecessarily.

Do not place a PCB on top of an anti-static bag. Only the inside of the bag is safe from static discharge.

4.2.2 Checklist

When CZGG LU-10-X is unpacked, please make sure the package contains the following items.

- 1 x CZGG LU-10-X CPU card
- 1 x Mini jumper pack
- 1 x IDE flat cable 40p/40p/40p
- 2 x SATA cables
- 1 x SATA power cable
- 1 x RS-232 cable
- 1x USB cable
- 1 x Audio cable
- 1 x KB/PS2 Mouse Y cable
- 1 x Utility CD

If one or more of these items are missing, please contact CyberResearch, Inc. and do not proceed further with the installation.

4.3 CZGG LU-10-X CPU Card Installation

WARNING!

Never run the CZGG LU-10-X without an appropriate heatsink and cooler that can be ordered from CyberResearch or purchased separately.

WARNING!

Please note that the installation instructions described in this manual should be carefully followed in order to avoid damage to the CZGG LU-10-X components and injury to the user.

WARNING!

When installing electronic components onto the CZGG LU-10-X always take the following anti-static precautions in order to prevent ESD damage to the CZGG LU-10-X and other electronic components like the CPU and DIMM modules

4.3.1 Preinstalled Components

The components listed below are preinstalled on the CZGG LU-10-X.

- CPU
- CPU heat sink

4.3.2 Components to Install

The following may already be completed by CyberResearch, Inc depending upon your order and/or system setup. Prior to installing the CZGG LU-10-X, the following components must be installed or connected first:

- DIMM modules

- Optional LCDC LVDS-LUKE-A daughterboard
- Peripheral devices

4.3.3 DIMM Module Installation

4.3.3.1 Purchasing the Memory Module

When purchasing DIMM modules, the following considerations should be taken into account: to 1GB of 333MHz or 400MHz of DDR memory

- The DIMM module can support a memory chip with a maximum size of 1GB
- The DIMM module can have a of 333MHz or 400MHz
- The DIMM can be either single-sided or dual-sided.

4.3.3.2 DIMM Module Installation

The CZGG LU-10-X CPU Card has two DDR SDRAM DIMM sockets. To install the DIMM modules, follow the instructions below and refer to ***Figure 4-1***.

Step 1: Pull the two white handles on either side of the DIMM socket down.

Step 2: Align the DIMM module with the DIMM socket making sure the matching pins are correctly aligned.

Step 3: Insert the DIMM module slowly. Once it is correctly inserted, push down firmly. The white handles on either side of the socket move back up and lock the module into the socket.

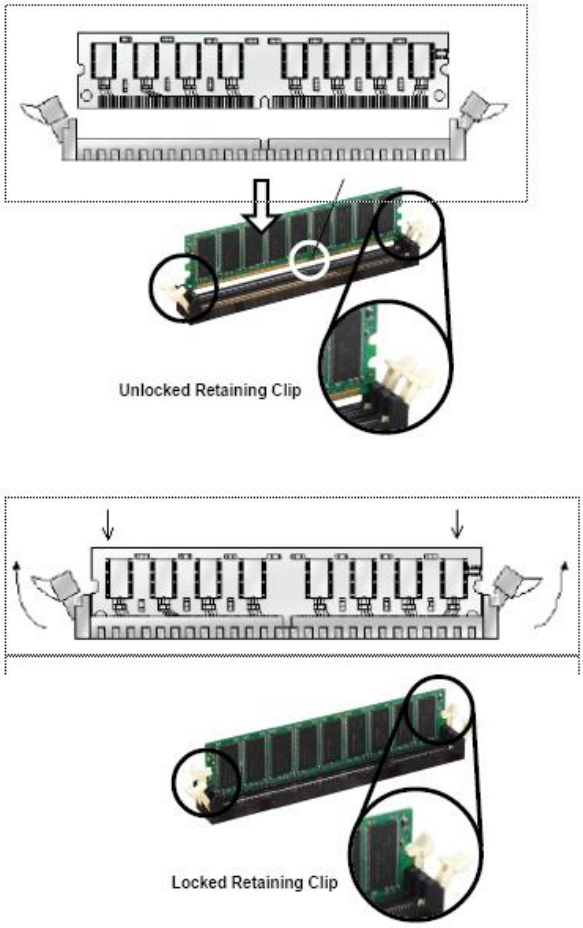

Figure 4-1: DIMM Module Installation

4.3.4 Optional LCDC LVDS-LUKE-A Daughterboard Installation

WARNING:

Installing the LCDC LVDS-LUKE-A daughterboard incorrectly may cause irreparable damage to the TTL display and the CZGG LU-10-X

The LCDC LVDS-LUKE-A daughterboard supports 18-bit and 24-bit TTL devices. The LCDC LVDS-LUKE-A daughterboard is installed on the J1 and J3 connectors. If 18-bit TTL connectivity is required, Pin 27 and Pin 28 on J1 and J3 must be left uncovered. If 24-bit TTL connectivity is required, Pin 1 and Pin 2 on J1 and J3 must be left uncovered. For further details see 4.3.4.1.

4.3.4.1 18-bit TTL Connectivity

To correctly install the LCDC LVDS-LUKE-A daughterboard to support an 18-bit TTL display, please follow the instructions below.

Step 1: Correctly orientate the LCDC LVDS-LUKE-A daughterboard. The VIA chipset on the LCDC LVDS-LUKE-A daughterboard should be on the side of the LCDC LVDS-LUKE-A facing the gold finger backplane connectors. The VIA chipset on the LCDC LVDS-LUKE-A should be on the side closest to the CPU.

Step 2: Align the connectors on the bottom of the LCDC LVDS-LUKE-A with pins 1 – pins 26 on the J1 and J3 connectors.

Step 3: Slide the LCDC LVDS-LUKE-A onto the connectors. Pin 27 and pin 28 on both the J1 and J3 connector should be visible. See **Figure 4-2**.

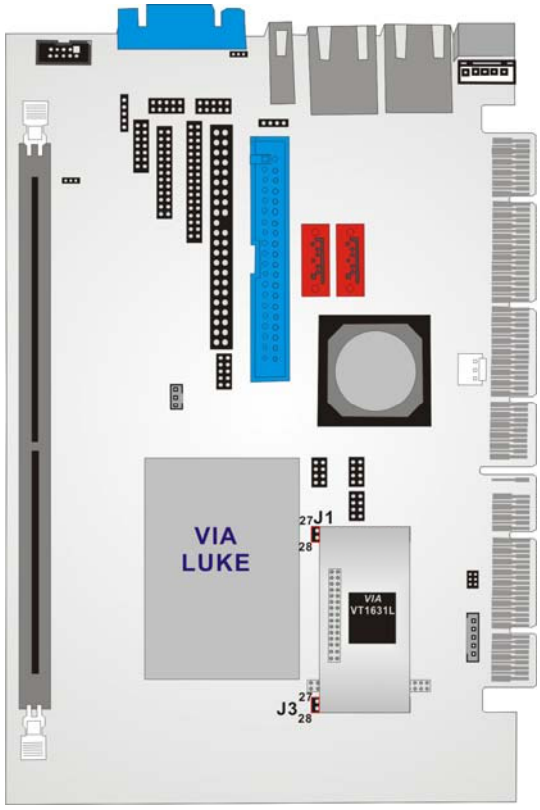

Figure 4-2: 18-bit TTL LCDC LVDS-LUKE-A Connectivity

4.3.4.2 24-bit TTL Connectivity

To correctly install the LCDC LVDS-LUKE-A daughterboard to support a 24-bit TTL display, please follow the instructions below.

Step 4: Correctly orientate the LCDC LVDS-LUKE-A daughterboard. The VIA chipset on the LCDC LVDS-LUKE-A daughterboard should on the side of the LCDC LVDS-LUKE-A facting the gold finger backplane connectors. The VIA chipset on the LCDC LVDS-LUKE-A should be on the side closest to the CPU.

Step 5: Align the connectors on the bottom of the LCDC LVDS-LUKE-A with pins 3 – pins 28 on the J1 and J3 connectors.

Step 6: Slide the LCDC LVDS-LUKE-A onto the connectors. Pin 1 and pin 2 on both the J1 and J3 connector should be visible. See **Figure 4-3**.

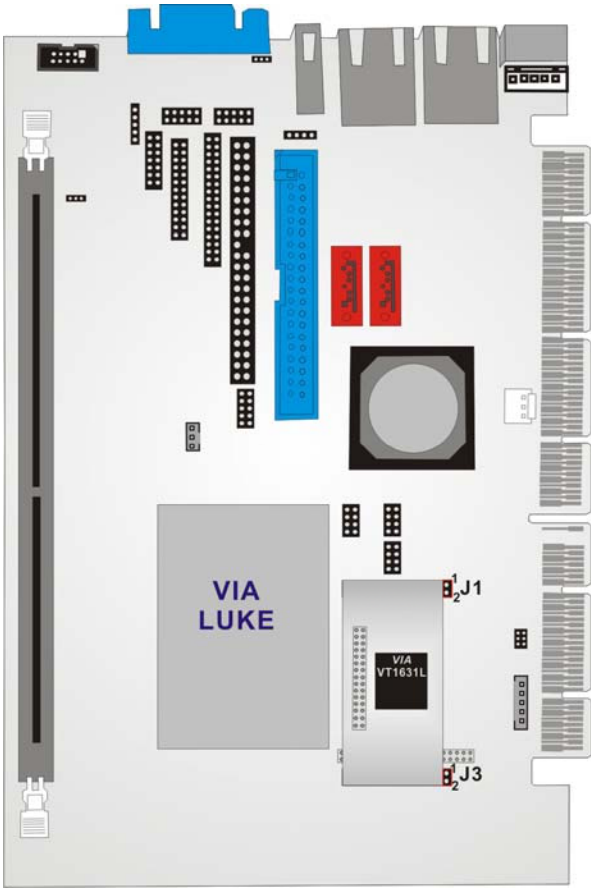

Figure 4-3: 24-bit TTL LCDC LVDS-LUKE-A Connectivity

4.3.5 Peripheral Device Connection

Cables provided by CyberResearch that connect peripheral devices to the board are listed in **Table 4-1**. Cables not included in the kit must be separately purchased.

Quantity	Type
1	mini jumper pack
1	ATA33 HDD cable
1	Power cable
1	RS-232 cable

Table 4-1: Cables Provided by CyberResearch

4.3.5.1 IDE Disk Drive Connector (IDE1)

The cable used to connect the CZGG LU-10-X to the IDE HDD is a standard 44-pin ATA33 flat cable. To connect an IDE device to the CZGG LU-10-X follow the instructions below.

Step 7: Find the ATA33 flat cable in the kit that came with the CZGG LU-10-X.

Step 8: Connect one end of the cable to the IDE1 connector on the CZGG LU-10-X. A keyed pin on the IDE connectors prevents it from being connected incorrectly.

Step 9: Locate the red wire on the other side of the cable that corresponds to the pin 1 connector.

Step 10: Connect the other side of the cable to the IDE device making sure that the pin 1 cable corresponds to pin 1 on the connector.

NOTE:

When two EIDE disk drives are connected together, back-end jumpers on the drives must be used to configure one drive as a master and the other as a slave.

4.3.5.2 Compact Flash Connector

The compact flash connector is located on the bottom of the daughter expansion board. If a user wishes to implement the CF connector for CD drive connectivity, please follow these instructions.

Step 1: Connect one end of a ribbon cable to the IDE2 connector on the CZGG LU-10-X CPU Card.

Step 2: Connect the other end of the same ribbon cable in Step 1 to the IDE1 connector on the expansion daughterboard.

4.4 Chassis Installation

After the DIMM modules have been installed and after the internal peripheral connectors have been connected to the peripheral devices and the jumpers have been configured, the CZGG LU-10-X can be mounted into chassis.

To mount a board into a chassis, please refer to the chassis user guide that came with the product.

4.5 Rear Panel Connectors

4.5.1 LCD Panel Connection

The conventional CRT monitor connector, VGA1, is a 15-pin, female D-SUB connector. It can be connected to an external monitor.

4.5.2 Ethernet Connection

The rear panel RJ-45 connectors can be connected to an external LAN and communicate with data transfer rates up to 100M/s.

4.5.3 USB Connection

The rear panel USB connectors provide easier and quicker access to external USB devices. The rear panel USB connector is a standard connector and can easily be connected to other USB devices.

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Chapter

5

AMI BIOS Setup

5.1 Introduction

A licensed copy of AMI BIOS is preprogrammed into the ROM BIOS. The BIOS setup program allows users to modify the basic system configuration. This chapter describes how to access the BIOS setup program and the configuration options are user configurable.

5.1.1 Starting Setup

The AMI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. Press the **DELETE** key as soon as the system is turned on or
2. Press the **DELETE** key when the "**Press Del to enter SETUP**" message appears on the screen.

If the message disappears before the user responds, restart the computer and try again.

5.1.2 Using Setup

Use the arrow keys to highlight items, press ENTER to select, use the PageUp and PageDown keys to change entries, press F1 for help and press ESC to quit. Navigation keys are shown in.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
Esc key	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
Page Up key	Increase the numeric value or make changes
Page Dn key	Decrease the numeric value or make changes
F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2 /F3 key	Change color from total 16 colors. F2 to select color forward.
F10 key	Save all the CMOS changes, only for Main Menu

Table 5-1: BIOS Navigation Keys

5.1.3 Getting Help

When F1 is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window press ESC or the F1 key again.

5.1.4 Unable to Reboot After Configuration Changes

If the computer is unable to boot after changes are made to the system configuration, restore the CMOS defaults. Use the jumper described in Chapter **Chapter 3**, **Section 3.4.1**.

5.1.5 BIOS Menu Bar

The menu bar on top of the BIOS screen has the following main items:

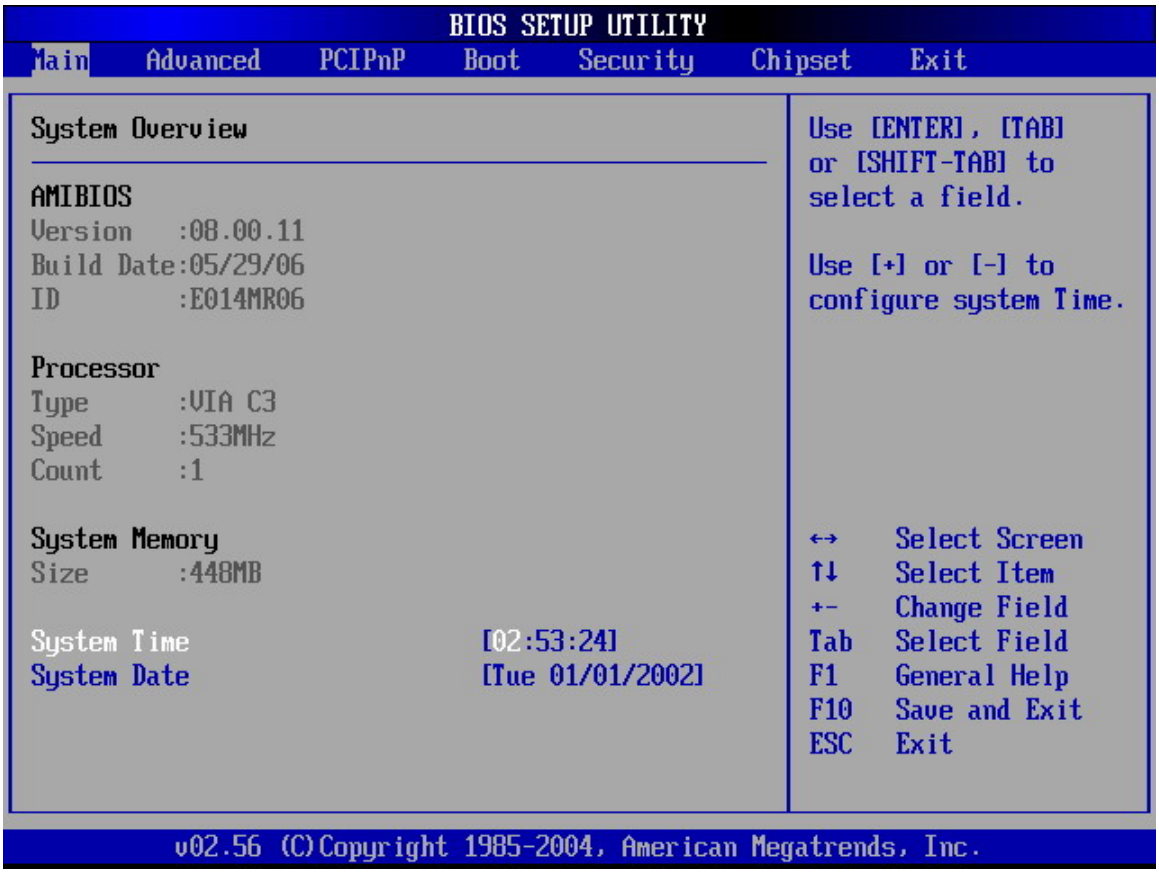
- **Main** Changes the basic system configuration.
- **Advanced** Changes the advanced system settings.
- **PCIPnP** Changes the advanced PCI/PnP Settings
- **Boot** Changes the system boot configuration.
- **Security** Sets User and Supervisor Passwords.
- **Chipset** Changes the chipset settings.
- **Power** Changes power management settings.
- **Exit** Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

5.2

5.3 Main

When entering the **BIOS Setup** program, the **Main** menu (**BIOS Menu 1**) appears. The **Main** menu gives overview of the basic system information.



BIOS Menu 1: Main

➔ **System Overview**

The System Overview lists a brief summary of different system components. The fields in System Overview cannot be changed. The items shown in the system overview include:

- **AMI BIOS**: Displays auto-detected BIOS information
  - **Version**: Current BIOS version
  - **Build Date**: Date the current BIOS version was made
  - **ID**: Installed BIOS ID

- **Processor**: Displays auto-detected CPU specifications
  - **Type**: Names the currently installed processor
  - **Speed**: Lists the processor speed
  - **Count**: The number of CPUs on the CZGG LU-10-X

- **System Memory**: Displays the auto-detected system memory.
  - **Size**: Lists memory size

The **System Overview** field also has two user configurable fields:

- **System Time [xx:xx:xx]**: Allows system time to be set.
- **System Date [Day xx/xx/xxxx]:** Allows the system date to be set.

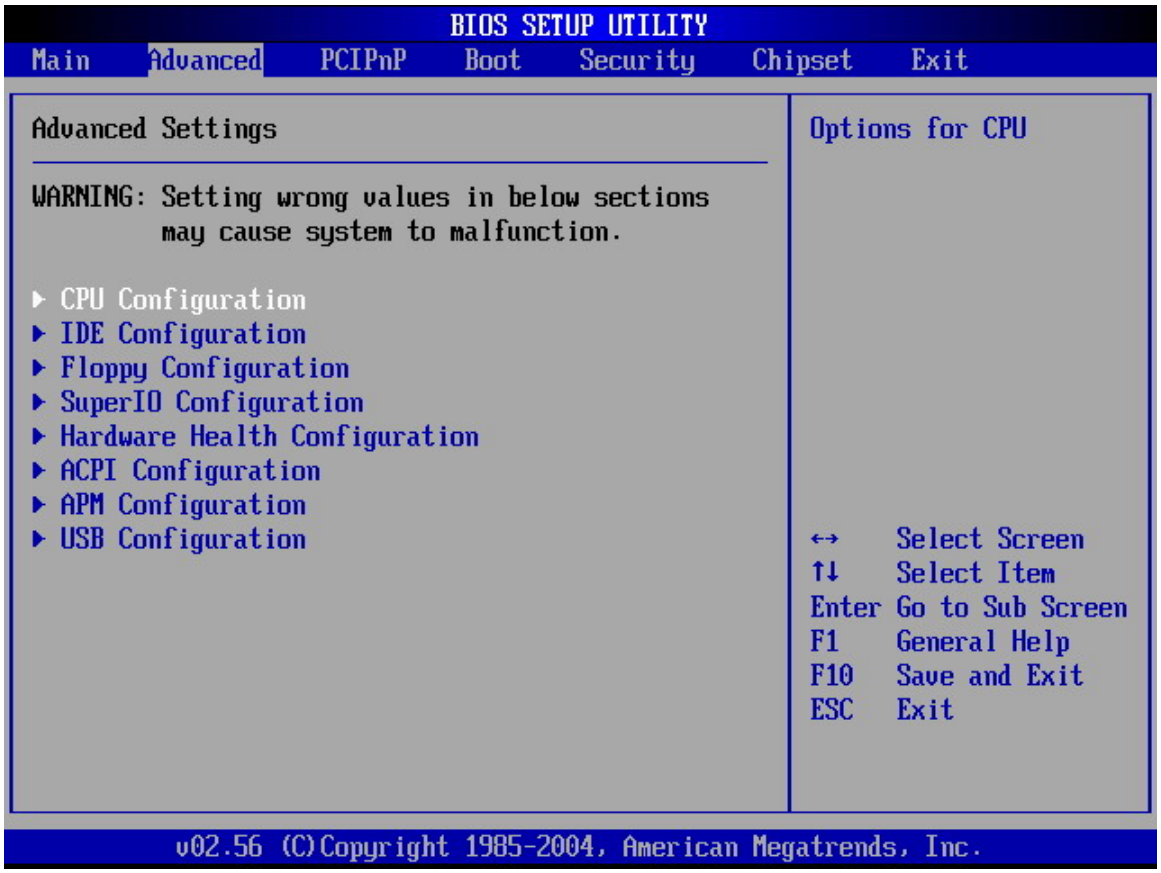
5.4 Advanced

The **Advanced** menu (**BIOS Menu 2**) allows CPU and peripheral device configuration options to be accessed through the following sub-menus:

WARNING:

Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings are compatible with the system hardware.

- CPU Configuration (see Section 5.4.1)
- IDE Configuration (see Section 5.4.2)
- Floppy Configuration (see Section 5.4.2)
- Super IO Configuration (see Section 5.4.3)
- Hardware Health Configuration (see Section 5.4.5)
- ACPI Configuration (see Section 5.4.6)
- APM Configuration (see Section 5.4.6.1)
- USB Configuration (see Section 5.4.8)



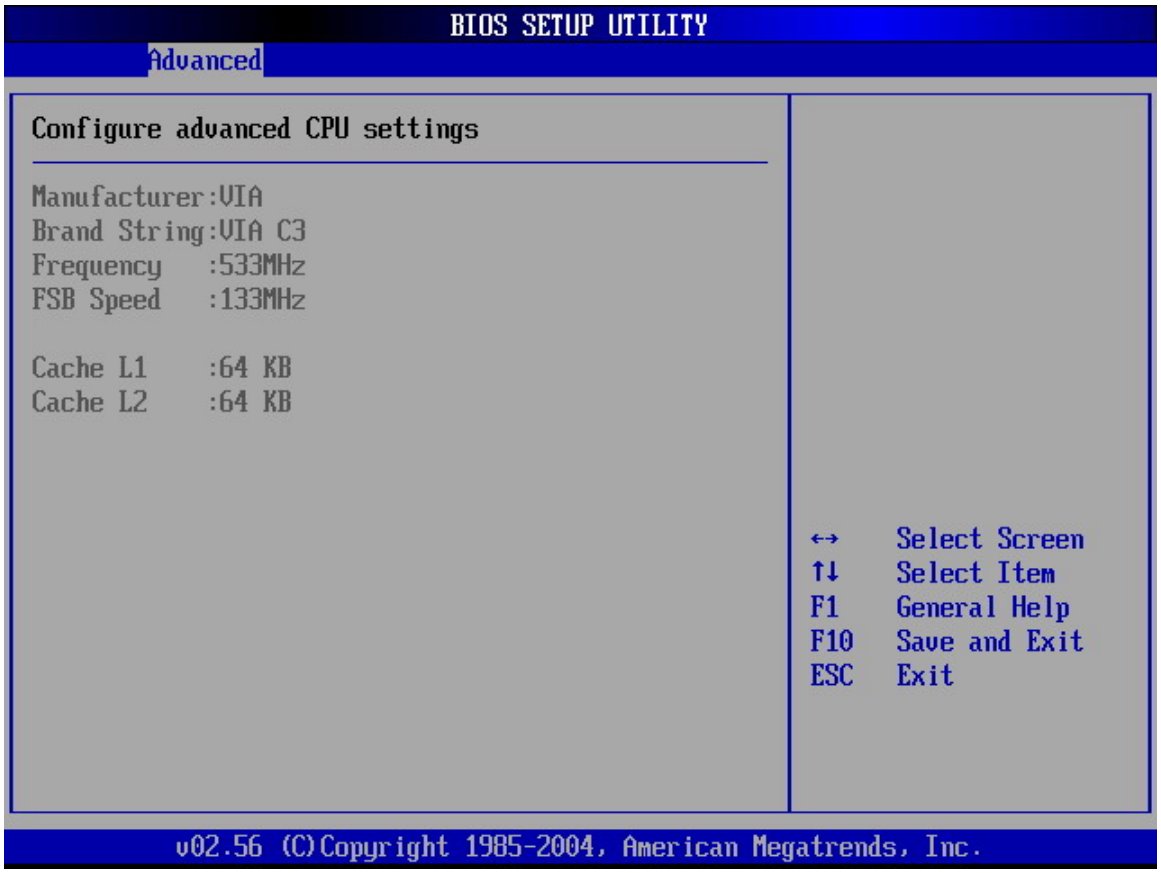
BIOS Menu 2: Advanced

NOTE:

The floppy configuration function shown in the menu above is not available on the CZGG LU-10-X.

5.4.1 CPU Configuration

The CPU Configuration menu (BIOS Menu 3) shows detailed CPU specifications.



BIOS Menu 3: CPU Configuration

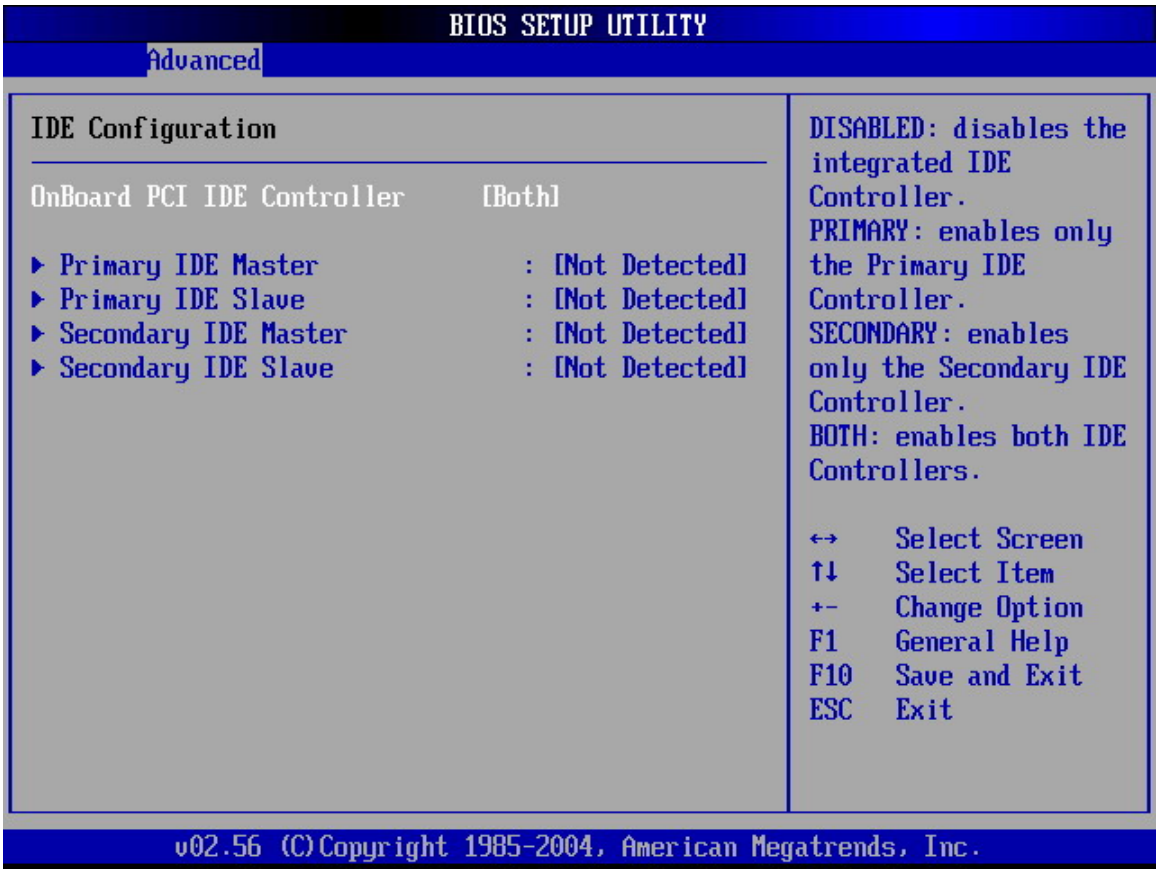
The CPU Configuration menu (BIOS Menu 3) lists the following CPU details:

- **Manufacturer**: Lists the name of the CPU manufacturer
- **Brand String**: Lists the brand name of the CPU being used
- **Frequency:** Lists the CPU processing speed
- **FSB Speed**: Lists the FSB speed
- **Cache L1**: Lists the CPU L1 cache size
- **Cache L2**: Lists the CPU L2 cache size (which in this case is zero)

The CPU Configuration menu (BIOS Menu 3) has two configurable parameters:

5.4.2 IDE Configuration

The IDE Configuration menu (BIOS Menu 4) IDE devices installed in the system to be user configured.



BIOS Menu 4: IDE Configuration

➔ **OnBoard PCI IDE Controller [Both]**

The **OnBoard PCI IDE Controller** BIOS option specifies the IDE channels used by the onboard PCI IDE controller. The following configuration options are available.

➔ **Disabled** Prevents the system from using the onboard IDE controller

➔ **Primary** Only allows the system to detect the Primary IDE channel, including both the Primary Master and Primary Slave)

➔ **Secondary** Only allows the system to detect the Secondary IDE channel, including both the Secondary Master and Secondary Slave)

➔ **Both** (Default) Allows the system to detect both the Primary and

Secondary IDE channels including the Primary Master, Primary Slave, Secondary Master and Secondary Slave.

➔ **IDE Master and IDE Slave**

When entering setup, BIOS auto detects the presence of IDE devices. This displays the status of the auto detected IDE devices. The following IDE devices are detected and are shown in the IDE Configuration menu:

- Primary IDE Master
- Primary IDE Slave
- Secondary IDE Master
- Secondary IDE Slave
- Third IDE Master
- Third IDE Slave

The **IDE Configuration** menu (**BIOS Menu 4**) changes the configurations for the IDE devices installed in the system. If an IDE device is detected, and one of the above listed four BIOS configuration options are selected, the IDE configuration options shown in **Section 5.4.2.1** appear.

➔ **Hard Disk Write Protect [Disabled]**

The **Hard Disk Write Protect** BIOS option protects hard disks from being overwritten. This menu item is only effective if the device is accessed through the BIOS.

➔	Disabled	(Default)	Allows hard disks to be overwritten
➔	Enabled		Prevents hard disks from being overwritten

➔ **IDE Detect Time Out (Sec) [35]**

The **IDE Detect Time Out (Sec)** BIOS option specifies the maximum time (in seconds) the AMI BIOS searches for IDE devices. This allows the settings to be fine-tuned and allows faster boot times. The following configuration options are available.

- 0 seconds
- 5 seconds (Default)
- 10 seconds
- 15 seconds
- 20 seconds

- 25 seconds
- 30 seconds
- 35 seconds

The best setting to use if the onboard IDE controllers are set to a specific IDE disk drive in the AMIBIOS is "0 seconds" and a large majority of ultra ATA hard disk drives can be detected well within "5 seconds."

➔ **ATA (PI) 80Pin Cable Detection [Host]**

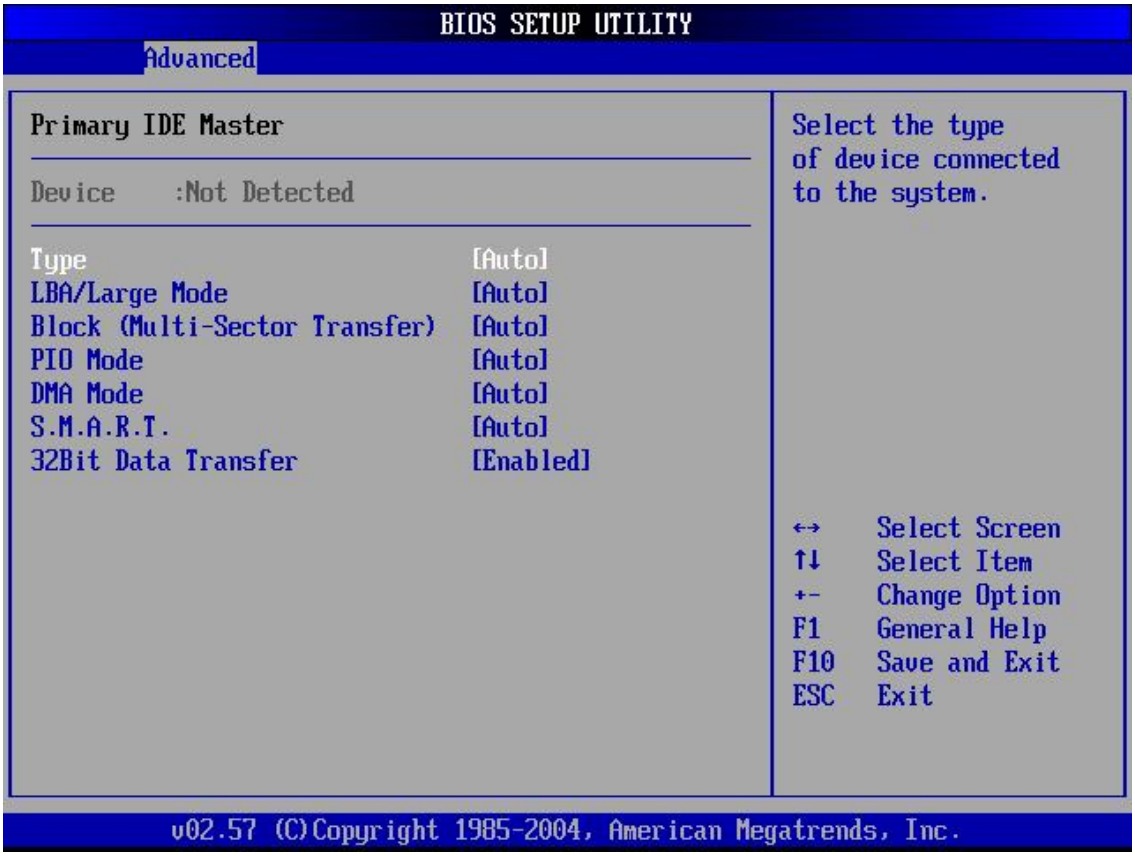
When an Ultra ATA/66, an Ultra ATA/100 or an Ultra ATA/133 IDE hard disk drive is used, an 80-conductor ATA cable must be used. The 80-conductor ATA cable is plug compatible with the standard 40-conductor ATA cable. The system must detect the presence of correct cable so that the AMI BIOS can instruct the drive to run at the correct speed for the cable type detected.

The **ATA (PI) 80Pin Cable Detection** BIOS option determines how the IDE cable is detected.

➔ **Host & Device**	(Default)	Both the CPU Card onboard IDE controller and IDE disk drive are used to detect the type of IDE cable used.
➔ **Host**		The CPU Card onboard IDE controller detects the type of IDE cable used.
➔ **Device**		The IDE disk drive detects the IDE cable type.

5.4.2.1 IDE Master, IDE Slave

IDE Master and IDE Slave configuration options for both primary and secondary IDE devices are shown in the BIOS menu below.



BIOS Menu 5: IDE Master and IDE Slave Configuration

➔ **Auto-Detected Drive Parameters**

The "grayed-out" items in the left frame are IDE disk drive parameters automatically detected from the firmware of the selected IDE disk drive. The drive parameters are listed as follows:

- **Device**: Lists the device type (e.g. hard disk, CD-ROM etc.)
- **Vendor**: Lists the device manufacturer
- **Size**: The size of the device.
- **LBA Mode**: Indicates whether the LBA (Logical Block Addressing) is a method of addressing data on a disk drive is supported or not.
- **Block Mode**: Block mode boosts IDE drive performance by increasing the amount of data transferred. Only 512 bytes of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 KB per interrupt.
- **PIO Mode**: Indicates the PIO mode of the installed device.
- **Async DMA**: Indicates the highest Asynchronous DMA Mode that is

supported.

- **Ultra DMA**: Indicates the highest Synchronous DMA Mode that is supported.
- **S.M.A.R.T.**: Indicates whether or not the Self-Monitoring Analysis and Reporting Technology protocol is supported.

➔ **Type [Auto]**

The **Type** BIOS option determines the type of device that the AMIBIOS attempts to boot from after the Power-On Self-Test (POST) has completed.

➔ **Not Installed** Selecting this value prevents the BIOS from searching for an IDE disk drive on the specified channel.

➔ **Auto** (Default) This selection enables the BIOS to auto detect the IDE disk drive type attached to the specified channel. This setting should be used if an IDE hard disk drive is attached to the specified channel.

➔ **CD/DVD** The CD/DVD option specifies that an IDE CD-ROM drive is attached to the specified IDE channel. The BIOS does not attempt to search for other types of IDE disk drives on the specified channel.

➔ **ARMD** This option specifies an ATAPI Removable Media Device. These include, but are not limited to:

- ➔ **ZIP**
- ➔ **LS-120**

➔ **LBA/Large Mode [Auto]**

The **LBA/Large Mode** BIOS option disables or auto detects LBA (Logical Block Addressing). LBA is a method of addressing data on a disk drive. In LBA mode, the maximum drive capacity is 137 GB.

➔ **Disabled** This selection prevents the BIOS from using the LBA mode control on the specified channel.

- ➔ **Auto** (Default) This option allows the BIOS to auto detect the LBA mode control on the specified channel.

➔ **Block (Multi Sector Transfer) [Auto]**

- ➔ **Disabled** Selecting this option prevents the BIOS from using Multi-Sector Transfer on the specified channel. The data to and from the device occurs one sector at a time.
- ➔ **Auto** (Default) Selecting this value to allows the BIOS to auto detect the device support for Multi-Sector Transfers on the specified channel. If supported. Select this value to allow the BIOS to auto detect the number of sectors per block for transfer from the hard disk drive to the memory. The data transfer to and from the device occurs multiple sectors at a time.

➔ **PIO Mode [Auto]**

The **PIO Mode** option selects the IDE PIO (Programmable I/O) mode program timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.

- ➔ **Auto** (Default) This setting allows the BIOS to auto detect the PIO mode. Use this value if the IDE disk drive support cannot be determined.
- ➔ **0** PIO mode 0 selected with a maximum transfer rate of 3.3MBps
- ➔ **1** PIO mode 1 selected with a maximum transfer rate of 5.2MBps
- ➔ **2** PIO mode 2 selected with a maximum transfer rate of 8.3MBps
- ➔ **3** PIO mode 3 selected with a maximum transfer rate of 11.1MBps
- ➔ **4** PIO mode 4 selected with a maximum transfer rate of 16.6MBps (This setting generally works with all hard disk drives manufactured after 1999. For other disk drives, such as IDE CD-ROM drives, check the specifications of the drive.)

➔ **DMA Mode [Auto]**

The **DMA Mode** BIOS selection allows adjusts the DMA mode options.

➔ **Auto** (Default) The BIOS auto detects the DMA mode. Use this value if the IDE disk drive support cannot be determined.

➔ **S.M.A.R.T [Auto]**

Self-Monitoring Analysis and Reporting Technology (**SMART**) feature can help predict impending drive failures. The S.M.A.R.T BIOS option enables or disables this function.

➔ **Auto** (Default) BIOS to auto detects if the hard disk drive supports S.M.A.R.T. Use this setting if the IDE disk drive support cannot be determined.

➔ **Disabled** Select this value to prevent the BIOS from using the SMART feature.

➔ **Enabled** Select this value to allow the BIOS to use the SMART feature on support hard disk drives.

➔ **32Bit Data Transfer [Enabled]**

The **32Bit Data Transfer** BIOS option enables or disables 32-bit data transfers.

➔ **Disabled** Prevents the BIOS from using 32-bit data transfers.

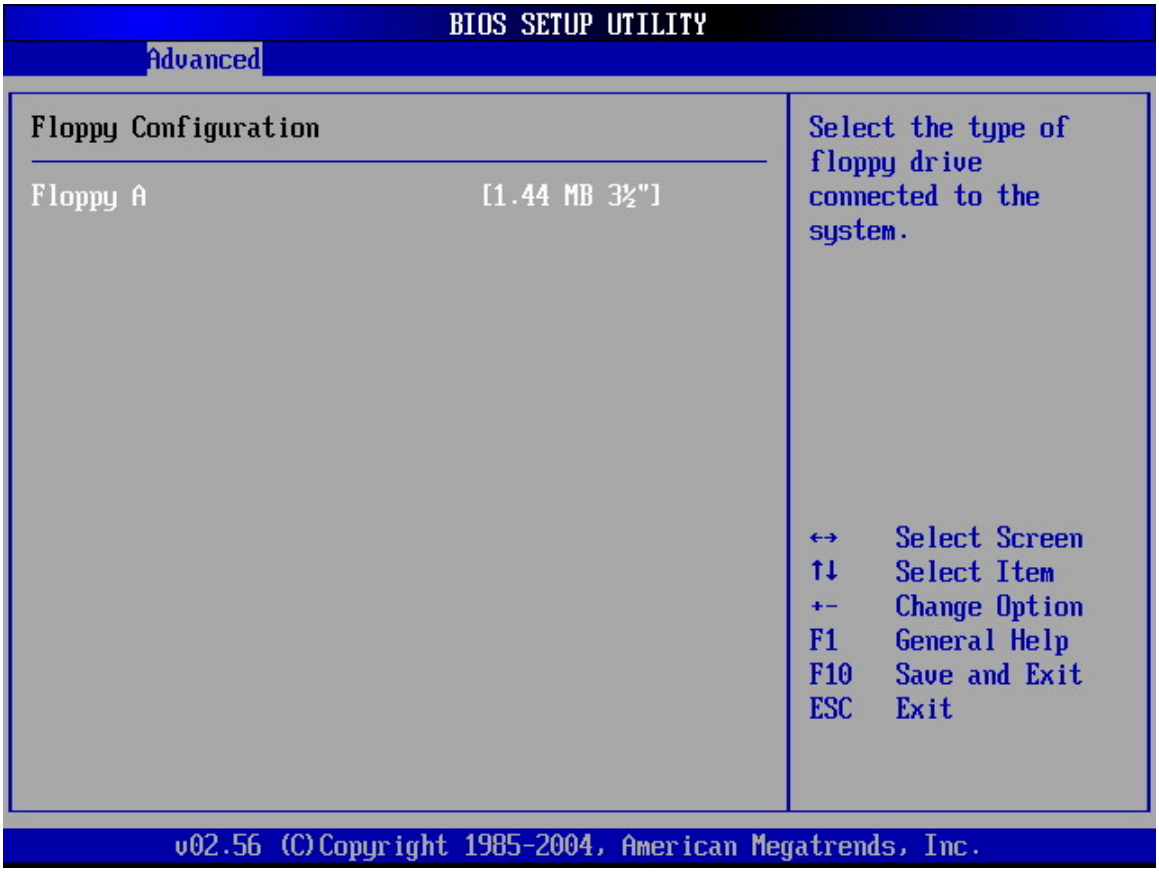
➔ **Enabled** (Default) Allows BIOS to use 32-bit data transfers on support hard disk drives.

5.4.3 Floppy Configuration

The **Floppy Configuration** menu (**BIOS Menu 6**) determines the type of floppy drive installed in the system. The Floppy Configuration menu has two configurable items: Floppy A and Floppy B. Both Floppy A and Floppy B have the same configuration options listed below.

- Disabled
- 360KB, 5.25 in

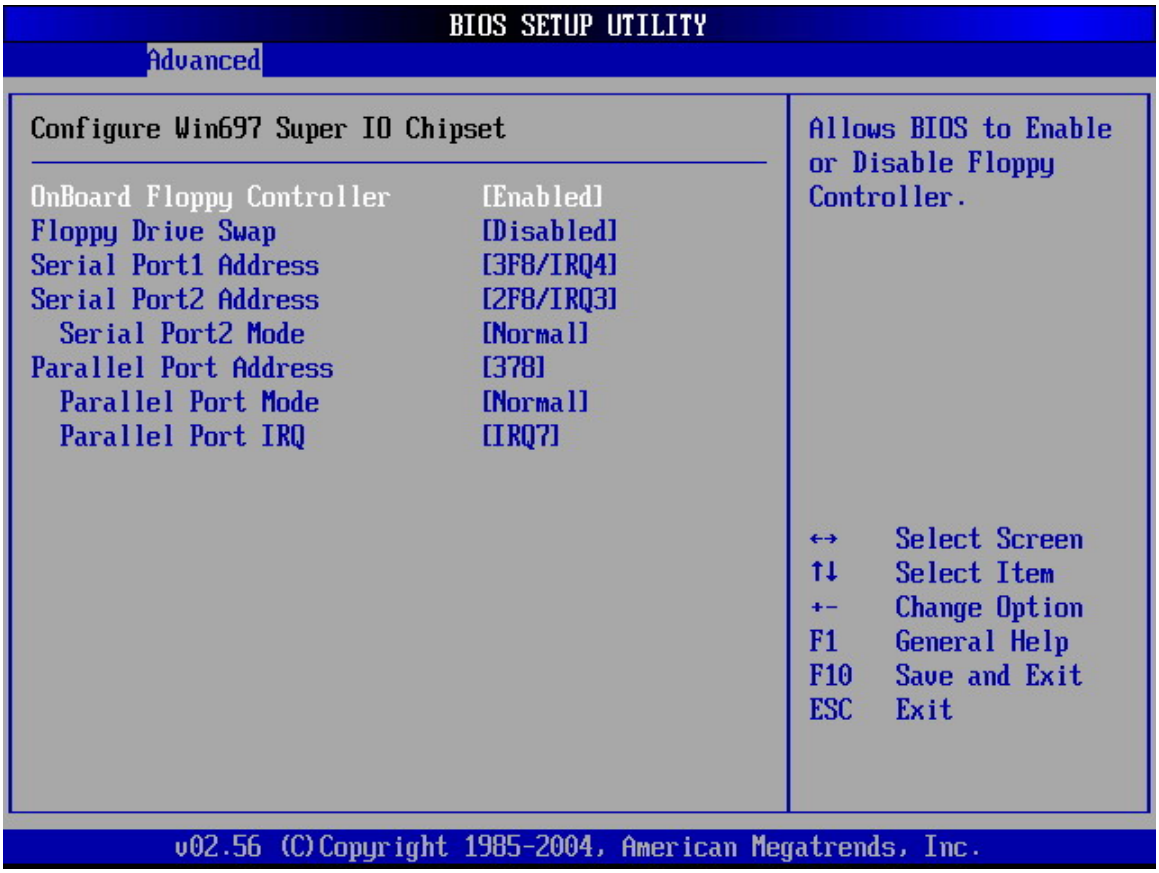
- 1.2MB, 5.25 in
- 720KB, 3.5 in
- 1.44MB, 3.5 in (Default)
- 2.88MB, 3.5in



BIOS Menu 6: Floppy Configuration

5.4.4 Super IO Configuration

The **Super IO Configuration** menu (**BIOS Menu 7**) sets or changes the configurations for the parallel ports and serial ports.



BIOS Menu 7: Super IO Configuration

➔ **On Board Floppy Controller [Enabled]**

The **OnBoard Floppy Controller** options enables or disables the floppy drive controller.

➔ **Disabled** Allows BIOS to disable the floppy controller

➔ **Enabled** (Default) Allows BIOS to enable the floppy controller

➔ **Floppy Drive Swap [Disabled]**

The **Floppy Drive Swap** option allows drive A to be designated as drive B and drive be to be designated as drive A.

➔ **Disabled** (Default) Cannot designate A or B to a floppy drive without changing the physical connection

➔ **Enabled** Can designate A or B to a floppy drive without changing the physical connection

➔ **Serial Port1 Address [3F8/IRQ4]**

The **Serial Port1 Address** option allows BIOS to select the Serial Port 1 base address.

➔ **Disabled**		No base address is assigned to Serial Port 1
➔ **3F8/IRQ4**	(Default)	Serial Port 1 I/O port address is 3F8 and the interrupt address is IRQ4
➔ **2F8/IRQ3**		Serial Port 1 I/O port address is 2F8 and the interrupt address is IRQ3
➔ **3E8/IRQ4**		Serial Port 1 I/O port address is 3E8 and the interrupt address is IRQ4
➔ **2E8/IRQ3**		Serial Port 1 I/O port address is 2E8 and the interrupt address is IRQ3

➔ **Serial Port2 Address [2F8/IRQ3]**

The **Serial Port2 Address** option allows BIOS to select the Serial Port 2 base address.

➔ **Disabled**		No base address is assigned to Serial Port 2
➔ **2F8/IRQ3**	(Default)	Serial Port 2 I/O port address is 2F8 and the interrupt address is IRQ3
➔ **3E8/IRQ4**		Serial Port 2 I/O port address is 3E8 and the interrupt address is IRQ4
➔ **2E8/IRQ3**		Serial Port 2 I/O port address is 2E8 and the interrupt address is IRQ3

➔ **Serial Port2 Mode [Normal]**

Allows BIOS to select the mode for Serial Port 2

➔ **Normal**	(Default)	Serial Port 1 mode is normal
➔ **IrDA**		Serial Port 1 mode is IrDA
➔ **ASK IR**		Serial Port 1 mode is ASK IR

➔ **Parallel Address [378]**

The **Parallel Port Address** BIOS option assigns the I/O port address of the parallel port. The following address options are available:

➔ **Disabled**		No I/O port address is assigned to the parallel port
➔ **378**	(Default)	Parallel Port I/O port address is 378
➔ **278**		Parallel Port I/O port address is 278
➔ **3BC**		Parallel Port I/O port address is 3BC

➔ **Parallel Port Mode [Normal]**

The **Parallel Port Mode** BIOS options selects the mode the parallel port operates in.

➔ **Normal**	(Default)	The normal parallel port mode is the standard mode for parallel port operation.
➔ **Bi-Directional**		Bi-Directional parallel port is able to receive 8 lines of data into the computer.
➔ **EPP**		The parallel port operates in the enhanced parallel port mode (EPP). The EPP mode supports bi-directional communication between the system and the parallel port device and the transmission rates between the two are much faster than the Normal mode.
➔ **ECP+EPP**		The parallel port operates in the extended capabilities port (ECP) mode. The ECP mode supports bi-directional communication between the system and the parallel port device and the transmission rates between the two are much faster than the Normal mode The parallel port becomes compatible with EPP devices described above

➔ **Parallel Port IRQ [IRQ7]**

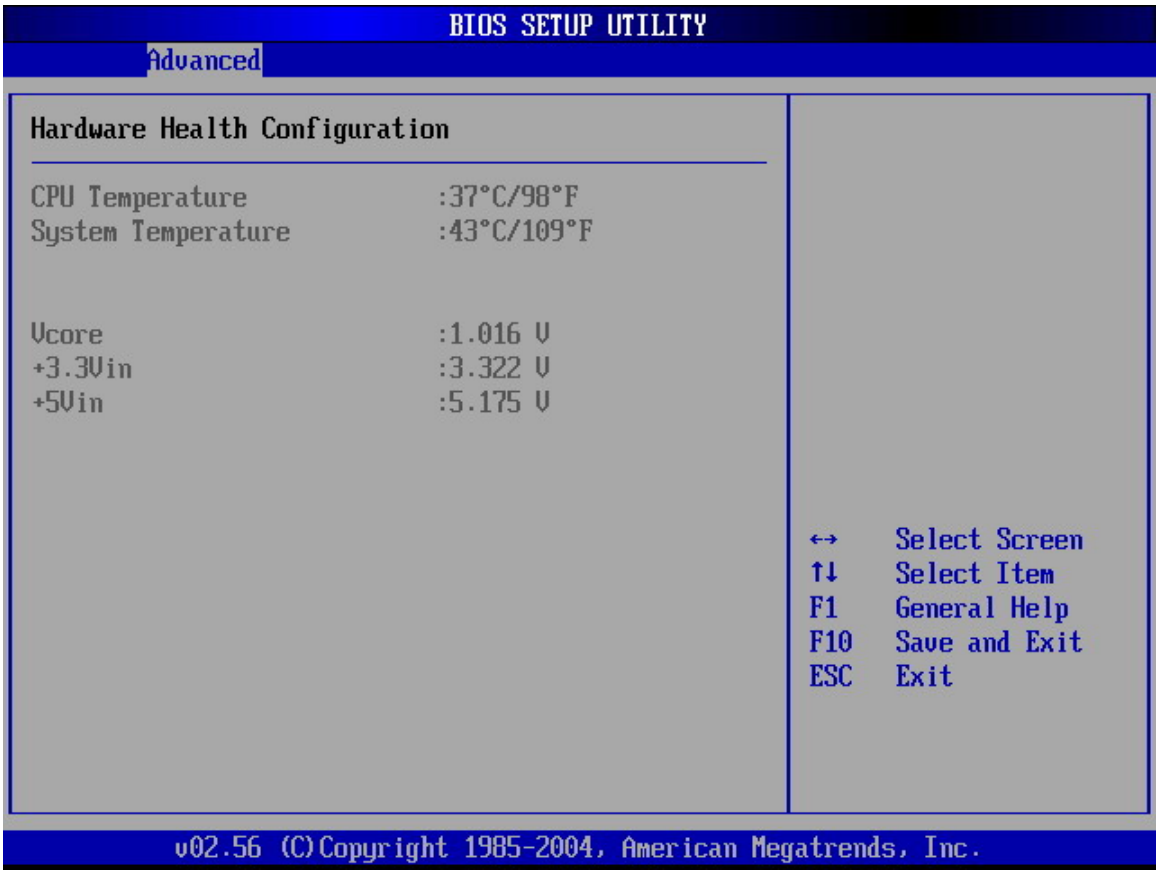
The **Parallel Port Address** BIOS option assigns the parallel port interrupt address. The following address options are available.

➔ **IRQ5** Parallel port interrupt address is IRQ5

➔ **IRQ7** (Default) Parallel port interrupt address is IRQ7

5.4.5 Hardware Health Configuration

The **Hardware Health Configuration** menu (**BIOS Menu 8**) shows the configuration for the H/W Health Function and shows the operating temperature and system voltages.



BIOS Menu 8: Hardware Health Configuration

➔ **H/W Health Function [Enabled]**

➔ **Disabled** Disables the health monitoring function

➔ **Enabled** (Default) Enables the health monitoring function

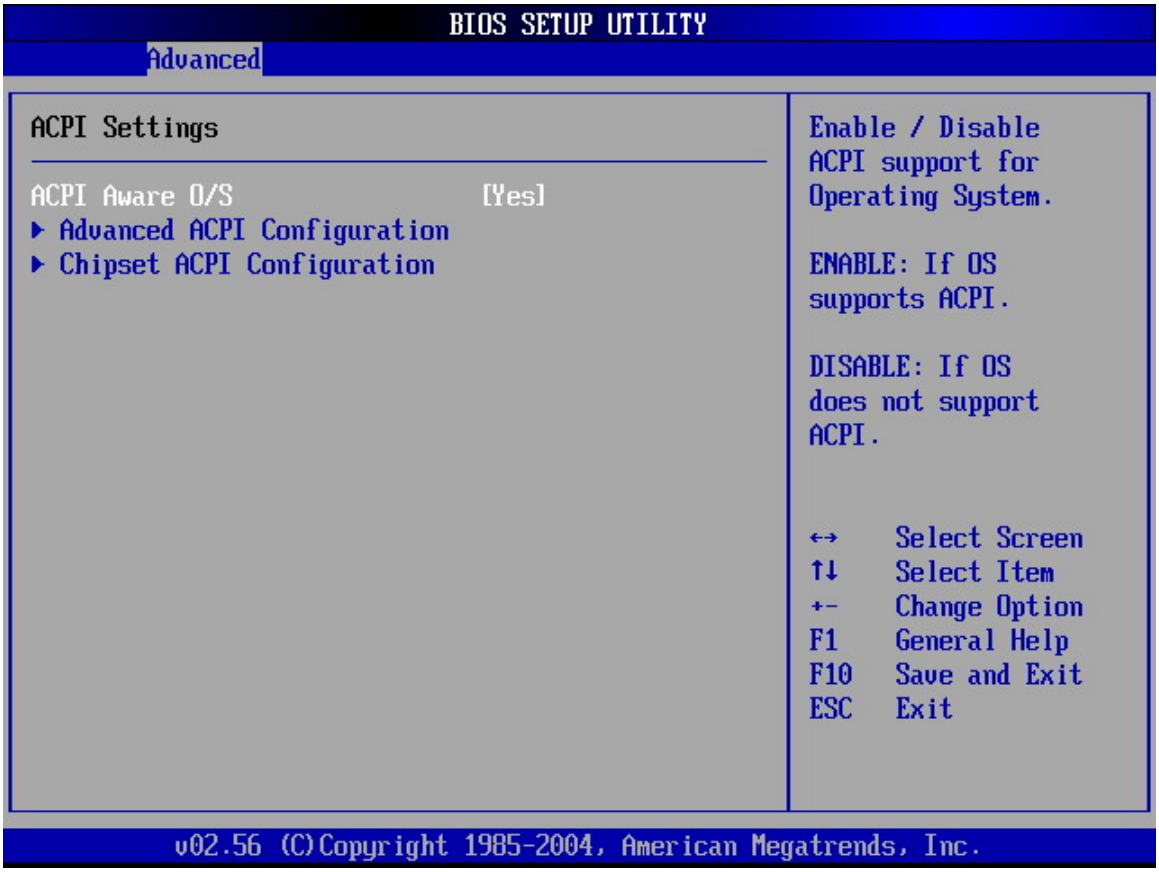
If the **H/W Health Function** is enabled different system parameters and values are shown. The following hardware health parameters are monitored.

- **System Temperatures**: The following system temperatures are monitored
  - CPU Temperature
  - System Temperature

- **Voltages**: The following system voltages are monitored
  - Vcore
  - +3.3Vin
  - +5Vin

5.4.6 ACPI Configuration

The **ACPI Configuration** menu (**BIOS Menu 9**) configures the Advanced Configuration and Power Interface (ACPI) and Power Management (APM) options.



BIOS Menu 9: ACPI Configuration

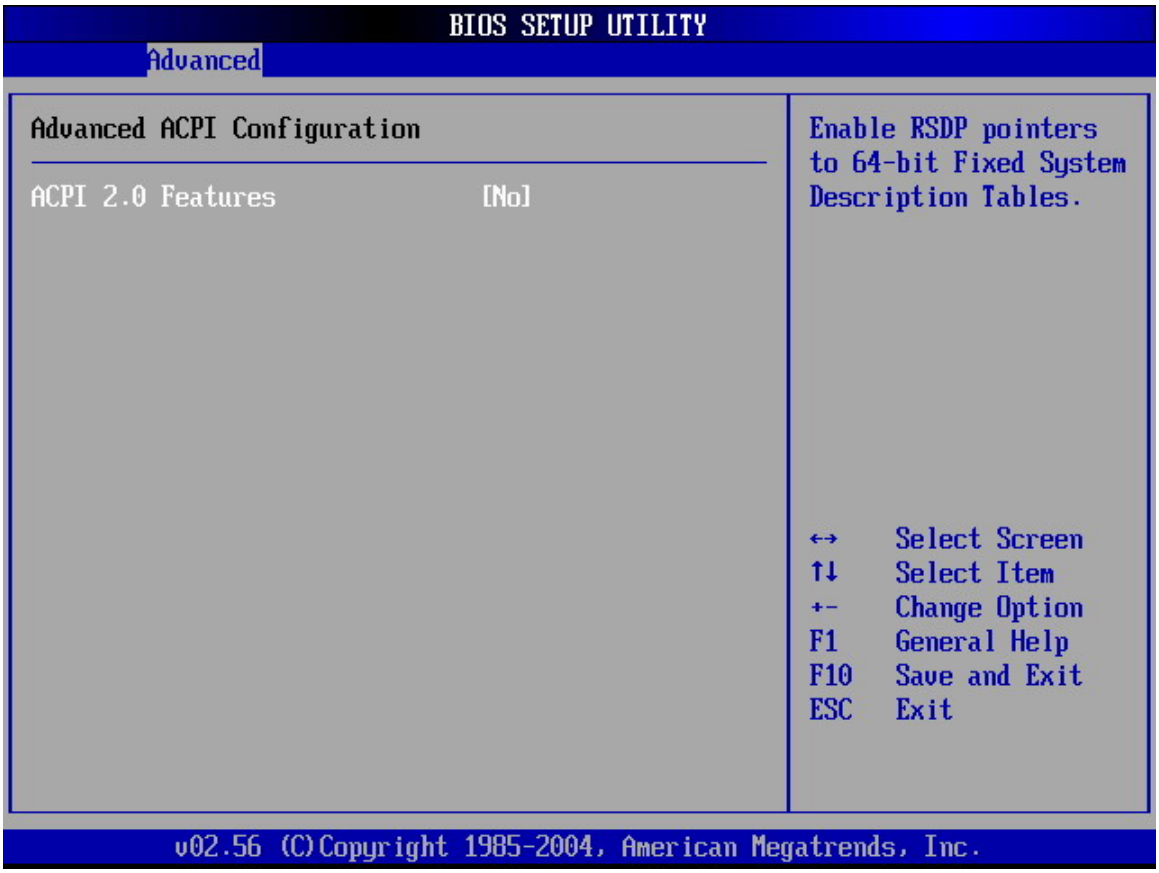
The following menu options appear in BIOS Menu 9:

- General ACPI Configuration

- Advanced ACPI Configuration
- Chipset ACPI Configuration

5.4.6.1 Advanced ACPI Configuration

The Advanced ACPI Configuration menu (BIOS Menu 10) selects the ACPI state when the system is suspended.



BIOS Menu 10: Advanced ACPI Configuration

➔ **ACPI 2.0 Features [No]**

The **ACPI 2.0 Features** BIOS enables the ACPI (Advanced Configuration and Power Interface) features. If enabled the system RSDP (Root System Description Pointer) can obtain physical addresses for other 64-bit fixed system description tables.

➔ **No** (Default) RSDP pointers to 64-bit fixed systems are not provided to the system

➔ **Yes** RSDP pointers to 64-bit fixed systems are provided to the

system

➔ **ACPI APIC Support [Enabled]**

The **ACPI APIC Support** BIOS option adds a pointer to an ACPI APIC table in the RSDT (Root System Description Table). The RSDT is an array of pointers that direct the system to the physical addresses of other description tables. The RSDT is the main ACPI table. The RSDP is located in low memory space of the system. It provides the physical address of the RSDT. The RSDT itself is identified in memory because it starts with the signature "RSDT."

➔ **Disabled** (Default) Pointers to the APIC APIC table are not be provided in the RSDT

➔ **Enabled** A pointers to the APIC APIC table are provided in the RSDT

➔ **AMI OEMB table [Enabled]**

The **AMI OEMB table** BIOS option adds a pointer to an OEMB table in the RSDT table and the Extended System Description Table (XSDT), which accommodates physical addresses of description headers that are larger than 32-bits. Notice that both the XSDT and the RSDT can be pointed to by the RSDP structure.

· ➔ **Disabled** (Default) Pointers to the AMI OEMB table are not provided in the RSDT and the XSDT

➔ **Enabled** Pointers to the AMI OEMB table are provided in the RSDT and the XSDT

➔ **Headless Mode [Disabled]**

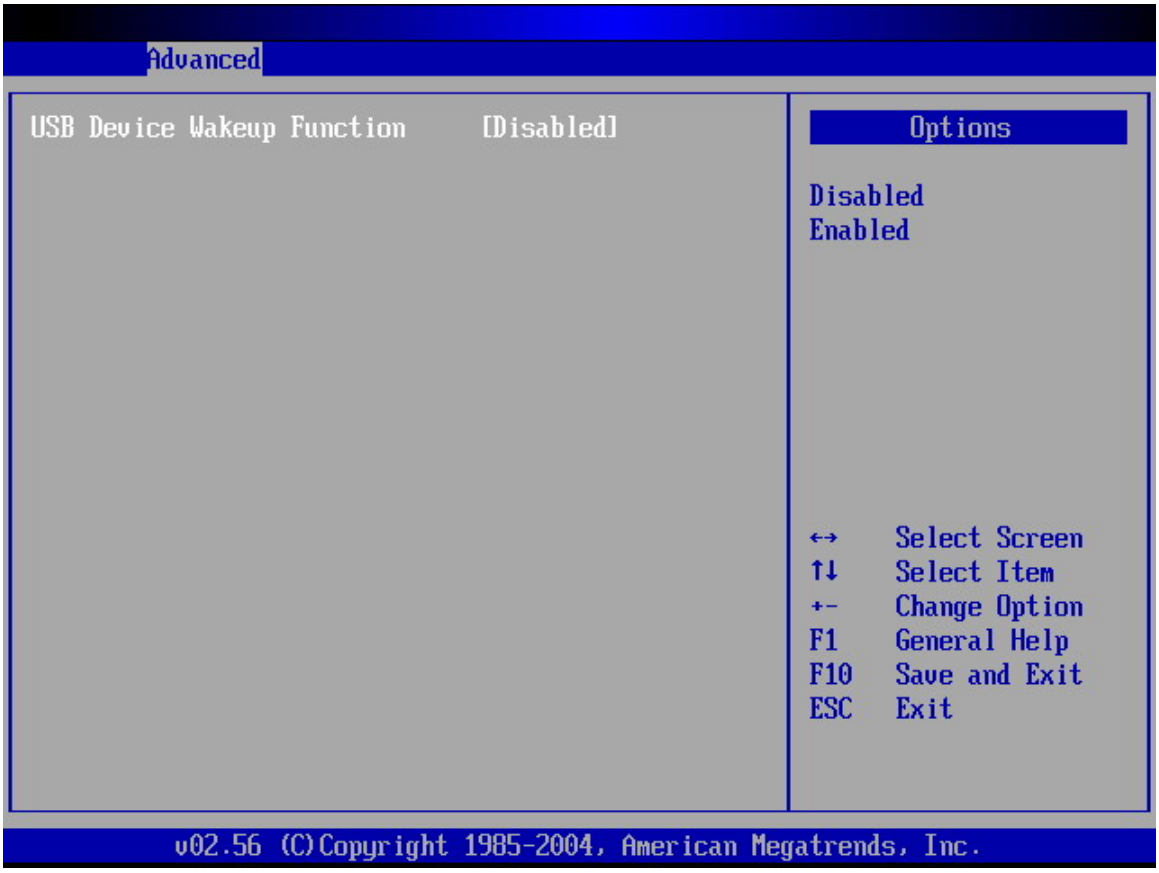
The **Headless Mode** to update the ACPI FACP (Fixed ACPI Description Table) indicates headless operations, i.e. a computer without a monitor, keyboard and mouse.

➔ **Disabled** (Default) The FACP is not updated to indicate headless mode

➔ **Enabled** The FACP is updated to indicate headless mode

5.4.6.2 Chipset ACPI Configuration

The Chipset ACPI Configuration menu (BIOS Menu 11) allows the USB to rouse a system from a sleep state or a suspend state.



BIOS Menu 11: Chipset ACPI Configuration

➔ **USB Device Wakeup Function [Enabled]**

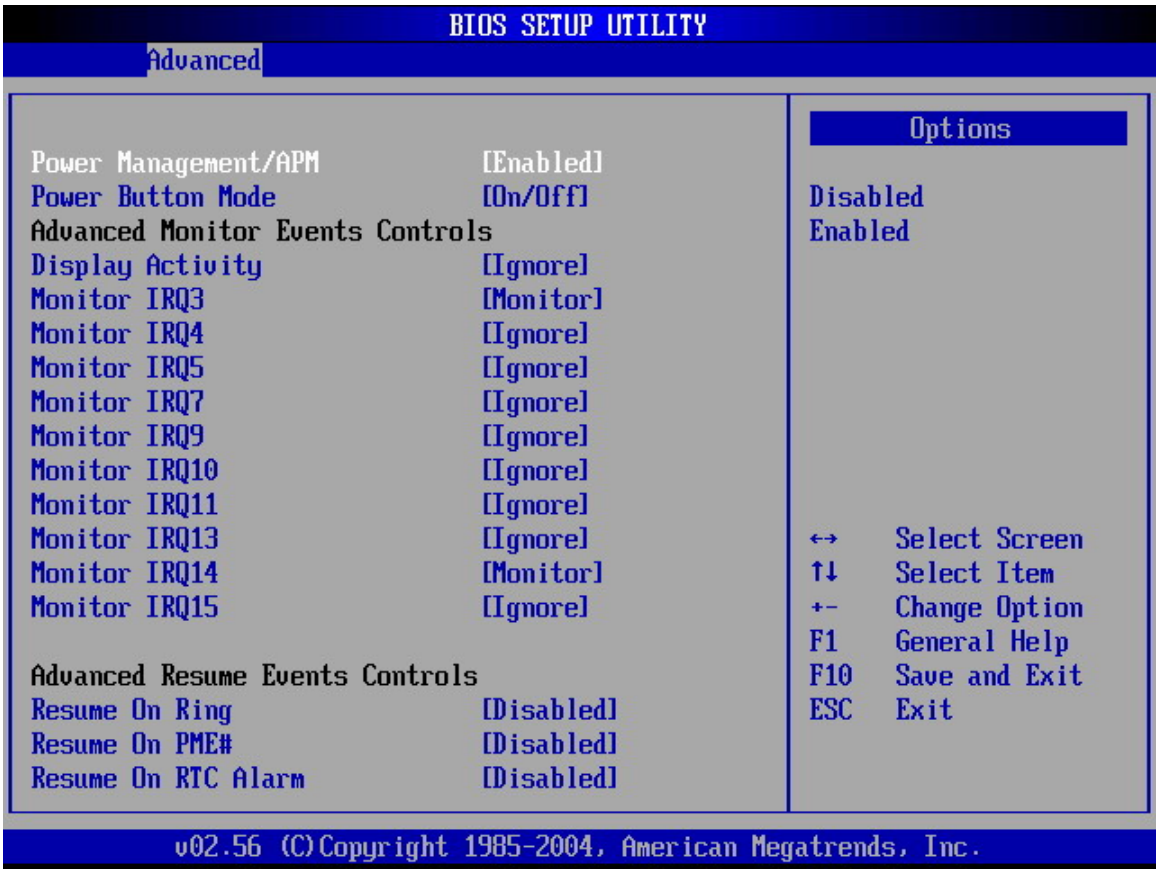
The **USB Device Wakeup** BIOS function enables activity on the USB device to rouse the system from a sleep state.

➔ **Disabled** Activity on the USB cannot rouse the system

➔ **Enabled** (Disable) Activity on the USB can rouse the system

5.4.7 APM Configuration

The APM Configuration menu (BIOS Menu 12) configures advanced power management options.



BIOS Menu 12: Power

➔ **Power Management/APM [Enabled]**

The **Power Management/APM** BIOS option provides access the advanced power management features.

➔ **Disabled** Disables the Advanced Power Management (APM) feature

➔ **Enabled** (Default) Enables the APM feature

➔ **Power Button Mode [On/Off]**

The **Power Button Mode** BIOS option specifies how the power button functions.

➔ **On/Off** (Default) When the power button is pressed the system is either turned on or off

➔ **Standby** When the power button is pressed the system goes into

standby mode

➔ **Suspend** When the power button is pressed the system goes into suspend mode

➔ **Display Activity [Ignore]**

The **Display Activity** BIOS option determines if activity on the Display is monitored or ignored. If activity is detected on the monitor, the system is activated from a suspended or sleep state.

➔ **Ignore** (Default) Activity is not monitored on the display

➔ **Monitor** Activity is not monitored on the display

➔ **Monitor IRQ#**

The **Monitor IRQ#** BIOS options specify the activity on IRQ# is monitored. If activity is monitored and detected on the specified IRQ, the system is roused from a suspended or sleep state.

➔ **Ignore** Activity is not monitored on the display

➔ **Monitor** Activity is not monitored on the display

Activity on the following IRQs can be monitored:

- IRQ3
- IRQ4
- IRQ5
- IRQ7
- IRQ9
- IRQ10
- IRQ11
- IRQ13
- IRQ14
- IRQ15

➔ **Resume on Ring [Disabled]**

The **Resume on Ring** BIOS specifies the system is roused from a suspended or standby state when there is activity on the RI (ring in) modem line. That is, the system is roused by an incoming call on a modem.

- ➔ **Disabled** (Default) Wake event not generated by an incoming call
- ➔ **Enabled** Wake event generated by an incoming call

➔ **Resume on Lan [Disabled]**

The **Resume on Lan** BIOS option specifies if the system is roused from a suspended or standby state when there is activity on the LAN.

- ➔ Disabled (Default) Wake event not generated by LAN activity
- ➔ Enabled Wake event generated by LAN activity

➔ **Resume on PME# [Disabled]**

The **Resume on PME#** BIOS option specifies if the system is roused from a suspended or standby state when there is activity on the PCI PME (power management event) controller.

- ➔ **Disabled** (Default) Wake event not generated by PCI PME controller activity
- ➔ **Enabled** Wake event generated by PCI PME controller activity

➔ **Resume on KBC [Disabled]**

The **Resume KBC** BIOS option specifies a keyboard key that can rouse a system from a suspended or standby state.

- ➔ **Disabled** (Default) No keyboard key specified
- ➔ **S3** The keyboard is used to rouse the system from an S3 Sleep state
- ➔ **S3/S4/S5** The keyboard is used to rouse the system from an S3, S4 or S5 Sleep state

➔ **Wake-Up Key**

The **Wake-up Key** BIOS option is only configurable if either **S3** or **S3/S4/S5** was selected above. This option specifies the key used to rouse the system.

- ➔ **Any Key** (Default) Any key can be used to rouse the system

➔ **Specific Key** If selected a Wake-Up password must be selected. The system can only be roused from the suspended state if the password is entered on the keyboard.

➔ **Resume on PS/2 Mouse [Disabled]**

The **PS/2 Mouse** BIOS option specifies if the system is roused from a suspended or standby state when there is activity on the PS/2 mouse.

➔ **Disabled** (Default) PS/2 mouse activity cannot rouse the system from a suspended stated.

➔ **S3** PS/2 mouse activity rouses the system from an S3 Sleep state

➔ **S3/S4/S5** PS/2 mouse activity rouses the system from an S3, S4 or S5 Sleep state

➔ **Resume On RTC Alarm [Disabled]**

The **Resume On RTC Alarm** determines when the computer is roused from a suspended state.

➔ **Disabled** (Default) The real time clock (RTC) cannot generate a wake event

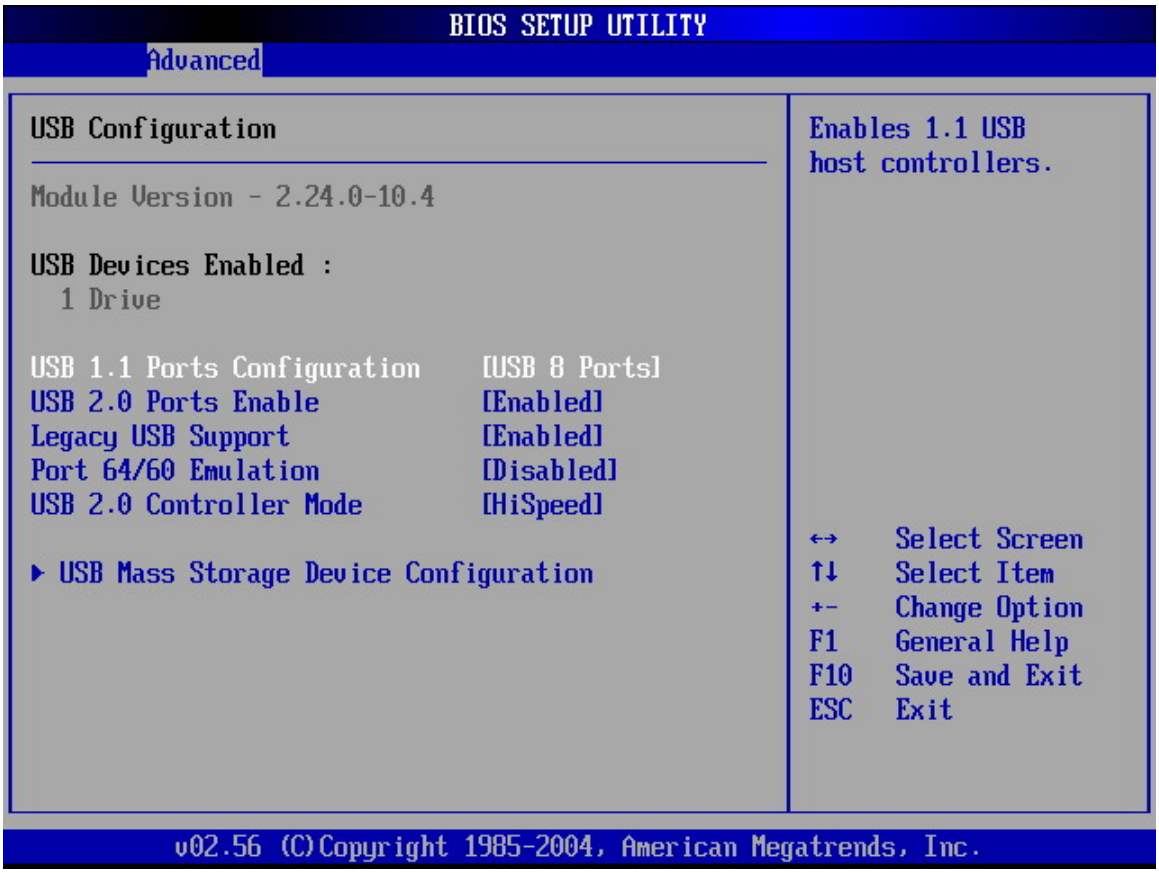
➔ **Enabled** If selected, the following appears with values that can be selected:

- ➔ **RTC Alarm Date (Days)**
- ➔ **System Time**

After setting the alarm, the computer turns itself on from a suspend state when the alarm goes off.

5.4.8 USB Configuration

The **USB Configuration** menu (**BIOS Menu 13**) gives information on the USB configuration and allows some USB features to be configured.



BIOS Menu 13: USB Configuration

➔ **USB Configuration**

The USB Configuration field shows the system USB configuration. The items listed are:

- Module Version: x.xxxxx.xxxxx

➔ **USB Devices Enabled:**

Lists the USB devices that are enabled on the system

➔ **USB 1.1 Ports Configuration [USB 8 Ports]**

The **USB Ports Configuration** BIOS option specifies how many of the USB ports are USB 1.1 compatible.

➔ **Disabled**	None of the ports are USB 1.1 compatible
➔ **USB 2 Ports**	Two ports are USB 1.1 compatible

- ➔ **USB 4 ports** Four ports are USB 1.1 compatible
- ➔ **USB 6 ports** Six ports are USB 1.1 compatible
- ➔ **USB 8 ports** (Default) Eight ports are USB 1.1 compatible

➔ **USB 2.0 Ports Enable [Enabled]**

The **USB 2.0 Ports** BIOS option enables or disables the USB 2.0 controller

- ➔ **Disabled** USB 2.0 function disabled
- ➔ **Enabled** (Default) USB 2.0 function enabled

➔ **Legacy USB Support [Disabled]**

The **Legacy USB Support** BIOS option refers to USB mouse and USB keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard does not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB driver loaded on the system.

- ➔ **Disabled** (Default) Legacy USB support disabled
- ➔ **Enabled** Legacy USB support enabled

➔ **Port 64/60 Emulation [Disabled]**

The **Port 64/60 Emulation Mode** BIOS option enables or disables the "Port 60h/64h" trapping option. Port 60h/64h trapping allows the BIOS to provide full PS/2 based legacy support for the USB keyboard and mouse. This option is useful for Microsoft Windows NT Operating System and for multi-language keyboards. Also this option provides the PS/2 functionalities like keyboard lock, password setting, scan code selection etc to USB keyboards.

- ➔ **Disabled** Port 60h/64h trapping option enabled
- ➔ **Enabled** (Default) Port 60h/64h trapping option disabled

➔ **USB2.0 Controller Mode [HiSpeed]**

The **USB2.0 Controller Mode** BIOS option sets the speed of the USB 2.0 controller.

➔ **FullSpeed** The controller is capable of operating at full speed (12Mbits/second)

➔ **HiSpeed** (Default) The controller is capable of operating at high speed (480Mbits/second)

➔ **BIOS EHCI Hand-Off [Enabled]**

The **BIOS EHCI** BIOS option enables support for Ises without EHCI hand-off support. The EHCI ownership change is claimed by the driver.

➔ **Disabled** EHCI Hand-Off not supported by BIOS

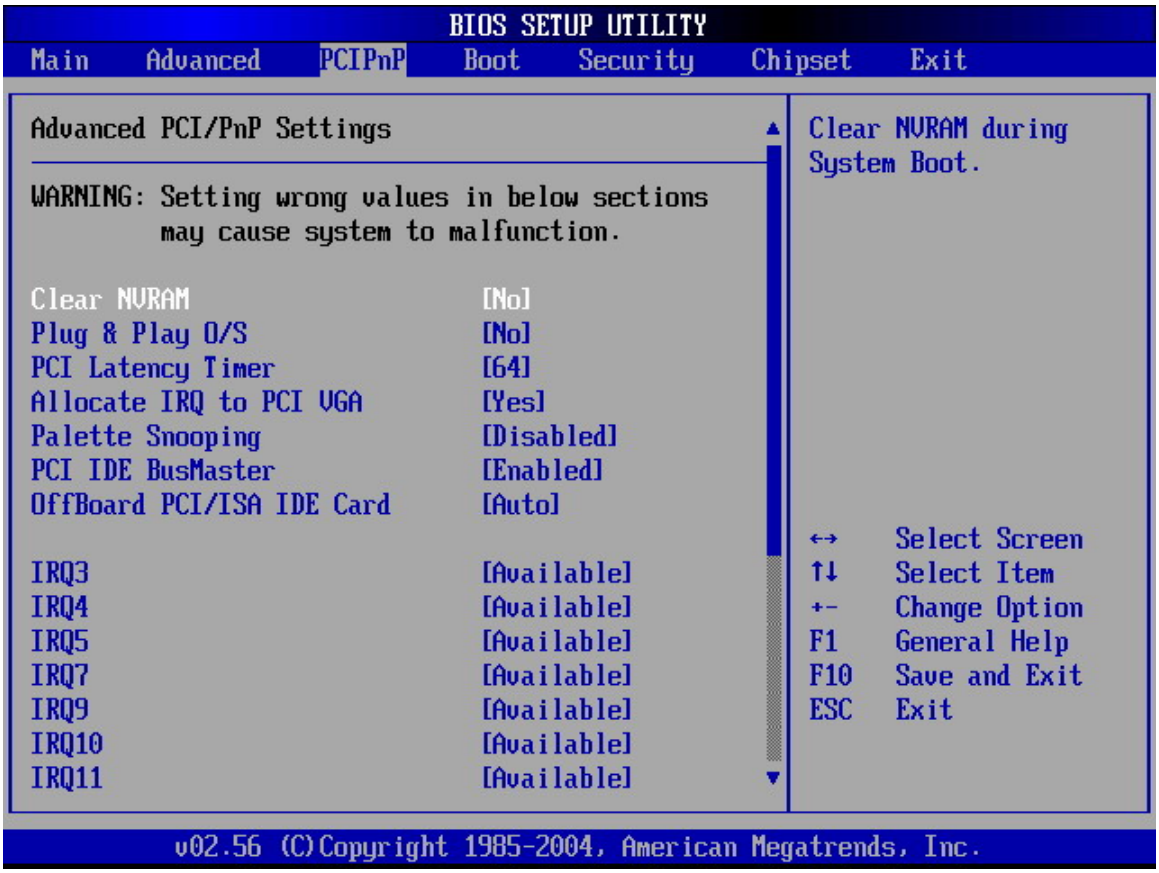
➔ **Enabled** (Default) EHCI Hand-Off supported by BIOS

5.5 PCI/PnP

The **PCI/PnP** menu (**BIOS Menu 13**) configures advanced PCI and PnP settings.

WARNING!

Setting incorrect values for the BIOS selections in the PCI PnP BIOS menu may cause system malfunctions.



BIOS Menu 14: PCI/PnP Configuration [Part 1]

➔ **Clear NVRAM [No]**

The **Clear NVRAM** specifies whether the contents of the NVRAM (Non-Volatile RAM) when the power is turned off.

➔ **No** (Default) System does not clear NVRAM during system boot

➔ **Yes** System clears NVRAM during system boot

➔ **Plug & Play O/S [No]**

The **Plug & Play O/S** BIOS determines whether the Plug and Play devices connected to the system are configured by the operating system or the BIOS.

➔ **No** (Default) If the operating system does not meet the Plug and Play specifications, this option allows the BIOS to configure all the devices in the system.

➔ **Yes** This setting allows the operating system to change the interrupt, I/O, and DMA settings. Set this option if the system is running Plug and Play aware operating systems.

➔ **PCI Latency Timer [64]**

The values stipulated in the **PCI Latency Timer** are in units of PCI clock cycles for the PCI device latency timer register. Configuration options are:

- 32
- 64 (Default)
- 96
- 128
- 160
- 192
- 224
- 248

➔ **Allocate IRQ to PCI VGA [Yes]**

The **Allocate IRQ to PCI VGA** restricted the system from giving the VGA adapter card an interrupt address.

➔ **Yes** (Default) Assigns an IRQ to a PCI VGA card if card requests IRQ

➔ **No** Does not assign IRQ to a PCI VGA card even if the card requests an IRQ

➔ **Palette Snooping [Disabled]**

The **Palette Snooping** enables or disables the palette snooping function.

➔ **Disabled** (Default) Unless the VGA card manufacturer requires palette snooping to be enabled, this option should be disabled.

➔ **No** PCI devices are informed that an ISA based Graphics device is installed in the system so the ISA based Graphics card functions correctly. This does not necessarily indicate a physical ISA adapter card. The

graphics chipset can be mounted on a PCI card. Always check with the adapter card manual first, before modifying the default settings in the BIOS.

➔ **PCI IDE BusMaster [Disabled]**

The **PCI IDE BusMaster** BIOS option enables or prevents the use of PCI IDE busmastering.

➔ **Disabled** (Default) Busmastering is prevented

➔ **No** IDE controller on the PCI local bus has mastering capabilities

➔ **OffBoard PCI/ISA IDE Card [Auto]**

The **OffBoard PCI/ISA IDE Card** BIOS option selects the OffBoard PCI/ISA IDE Card.

➔ **Auto** (Default) The location of the Off Board PCI IDE adapter card is automatically detected by the AMIBIOS.

➔ **PCI Slot 1** PCI Slot 1 is selected as the location of the OffBoard PCI IDE adapter card. Only select this slot if the adapter card is installed in PCI Slot 1.

➔ **PCI Slot 2** PCI Slot 2 is selected as the location of the OffBoard PCI IDE adapter card. Only select this slot if the adapter card is installed in PCI Slot 2.

➔ **PCI Slot 3** PCI Slot 3 is selected as the location of the OffBoard PCI IDE adapter card. Only select this slot if the adapter card is installed in PCI Slot 3.

➔ **PCI Slot 4** PCI Slot 4 is selected as the location of the OffBoard PCI IDE adapter card. Only select this slot if the adapter card is installed in PCI Slot 4.

➔ **PCI Slot 5** PCI Slot 5 is selected as the location of the OffBoard

PCI IDE adapter card. Only select this slot if the adapter card is installed in PCI Slot 5.

➔ **PCI Slot 6** PCI Slot 6 is selected as the location of the OffBoard PCI IDE adapter card. Only select this slot if the adapter card is installed in PCI Slot 6.

➔ **IRQ# [Available]**

➔ **Available** (Default) The specified IRQ is available to be used by PCI/PnP devices

➔ **Reserved** The specified IRQ is reserved for use by Legacy ISA devices

Available IRQ addresses are:

- IRQ3
- IRQ4
- IRQ5
- IRQ7
- IRQ9
- IRQ10
- IRQ 11
- IRQ 14
- IRQ 15

➔ **DMA Channel# [Available]**

➔ **Available** (Default) The specified DMA is available to be used by PCI/PnP devices

➔ **Reserved** The specified DMA is reserved for use by Legacy ISA devices

Available DMA Channels are:

- DM Channel 0
- DM Channel 1
- DM Channel 3

- DM Channel 5
- DM Channel 6
- DM Channel 7

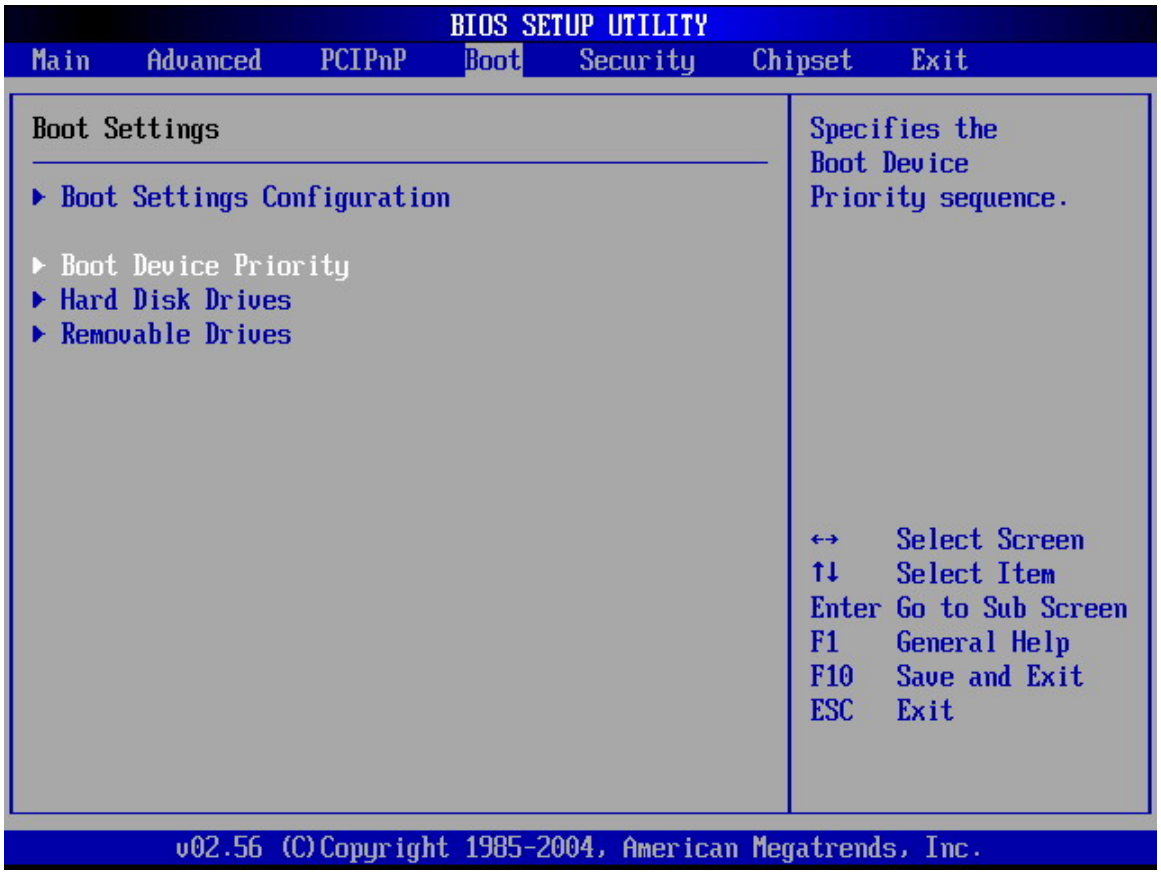
➔ **Reserved Memory Size [Disabled]**

The **Reserved Memory Size** BIOS option specifies the amount of memory that should be reserved for legacy ISA devices.

➔	**Disabled**	(Default)	No memory block reserved for legacy ISA devices
➔	**16K**		16KB reserved for legacy ISA devices
➔	**32K**		32KB reserved for legacy ISA devices
➔	**64K**		54KB reserved for legacy ISA devices

5.6 Boot

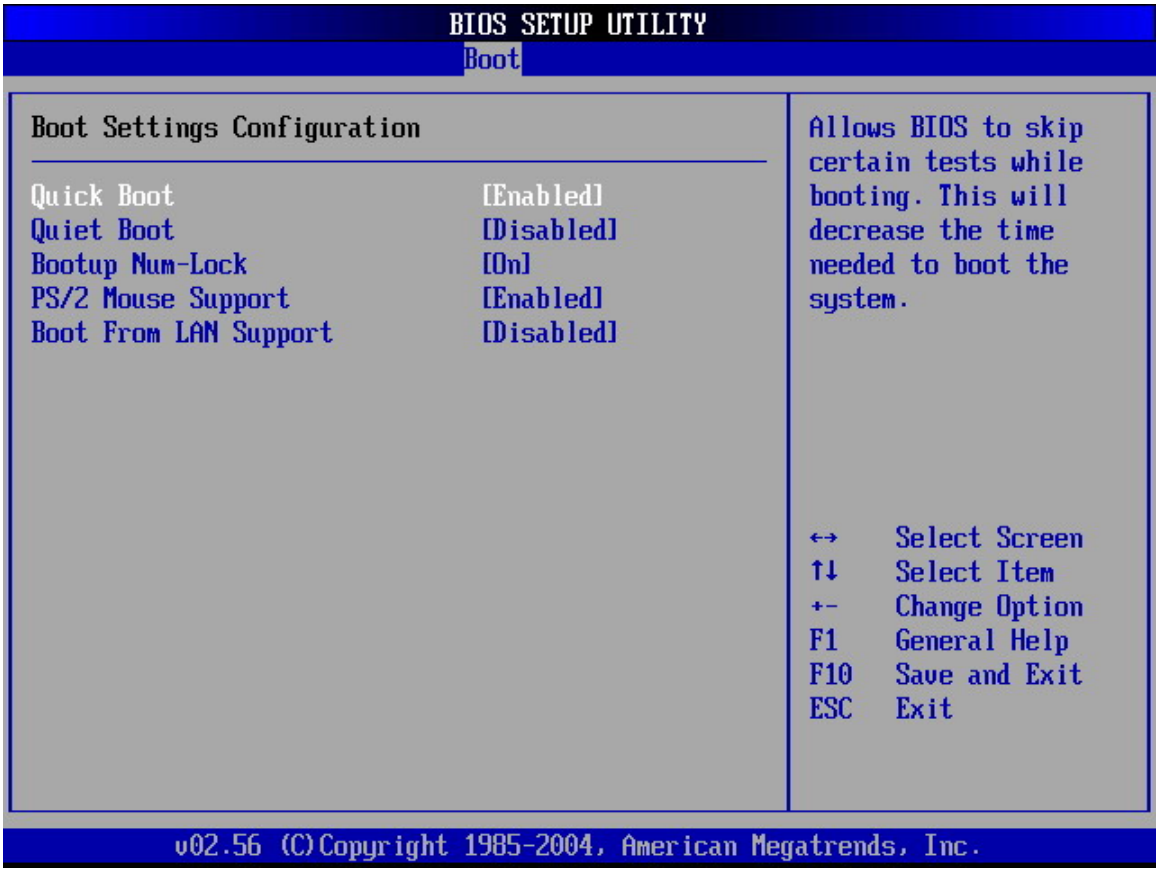
The Boot menu (BIOS Menu 15) configures system boot options.



BIOS Menu 15: Boot

5.6.1 Boot Settings Configuration

The Boot Settings Configuration menu (BIOS Menu 15) configures advanced system boot options.



BIOS Menu 16: Boot Settings Configuration

➔ **Quick Boot [Enabled]**

The **Quick Boot** BIOS option speeds up the boot process.

➔ **Disabled** System does not skip any POST procedures

➔ **Enabled** (Default) Allows system to skip some POST procedures to decrease the system boot time

➔ **Quiet Boot [Disabled]**

The **Quiet Boot** BIOS option allows the boot up screen options to be modified between POST messages or an OEM logo.

- ➔ **Disabled** (Default) Displays normal POST messages
- ➔ **Enabled** Displays OEM Logo instead of POST messages

➔ **AddOn ROM Display Mode [Force BIOS]**

The **AddOn ROM Display Mode** option allows add-on ROM (read-only memory) messages to be displayed.

- ➔ **Force BIOS** (Default) Allows the computer system to force a third party BIOS to display during system boot.
- ➔ **Keep Current** Allows the computer system to display the information during system boot.

➔ **Bootup Num-Lock [Off]**

The **Bootup Num-Lock** BIOS option allows the Number Lock setting to be modified during boot up.

- ➔ **Off** (Default) Does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard lights up when the Number Lock is engaged.
- ➔ **On** Allows the Number Lock on the keyboard to be enabled automatically when the computer system boots up. This allows the immediate use of the 10-key numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard is lit.

➔ **PS/2 Mouse Support [Enabled]**

The **PS/2 Mouse Support** BIOS option allows the PS/2 mouse support to be adjusted.

➔ **Disabled** Disables PS/2 mouse support and prevents the PS/2 mouse port from using system resources.

➔ **Enabled** Allows the system to use a PS/2 mouse.

➔ **Auto** (Default) Allows the system to automatically detect if a PS/2 mouse is being used.

➔ **Wait For 'F1' If Error [Enabled]**

The **Wait For 'F1' if Error** option specifies how the system responds when the system detects an error on boot up.

➔ **Disabled** If there is an error when booting up, the system does not wait for user intervention but continues to boot up in the operating system. Only use this setting if there is a known reason for a BIOS error to appear. An example would be a system administrator must remote boot the system. The computer system does not have a keyboard currently attached.

➔ **Enabled** (Default) If there is an error during boot up, the system waits for a user to press "F1" and enter the BIOS to rectify the problem. The BIOS can then be adjusted to the correct settings.

➔ **Hit 'DEL' Message Display [Enabled]**

The **Hit "DEL" Message Display** option specifies whether the instruction to hit the delete button to enter BIOS during POST appears or not.

➔ **Disabled** No message displayed during POST

➔ **Enabled** (Default) Displays "Press DEL to run Setup" message in POST

➔ **Interrupt 19 Capture [Disabled]**

The **Interrupt 19 Capture** ROM BIOS option allows optional ROMs such as network controllers to trap BIOS interrupt 19.

➔ **Disabled** (Default) Does not allow optional ROM to trap interrupt 19

➔ **Enabled** Allows optional ROM to trap interrupt 19

➔ **Boot From LAN Support [Disabled]**

The **BOOT From LAN Support** option enables the system to be booted from a remote system.

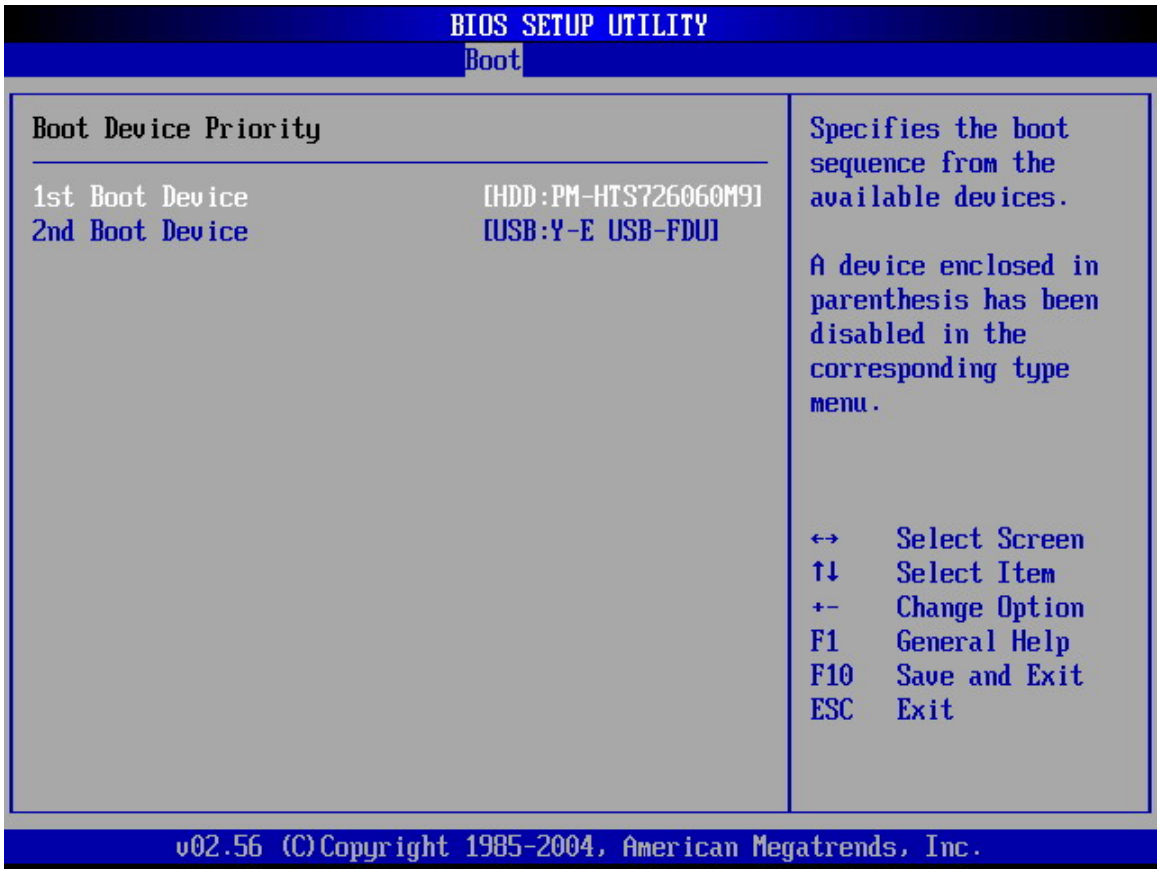
➔ **Disabled** (Default) Cannot be booted from a remote system through the LAN

➔ **Enabled** (Default) Can be booted from a remote system through the LAN

5.6.2 Boot Device Priority

The **Boot Device Priority** menu (**BIOS Menu 17**) specifies the boot sequence from the available devices. Possible boot devices may include:

- FDD
- HDD
- CD/DVD



BIOS Menu 17: Boot Device Priority

5.6.3 Hard Disk Drives

The **Hard Disk Drives** menu is similar to the **Removable Drives BIOS Menu 18** and it specifies the boot sequence of the available HDDs. When the menu is opened, the HDDs connected to the system are listed as shown below:

- 1st Drive [HDD: PM-(part number)]
- 2nd Drive [HDD: PS-(part number)]
- 3rd Drive [HDD: SM-(part number)]
- 4th Drive [HDD: SM-(part number)]

NOTE:

Only the drives connected to the system are not shown. For example, if

only two HDDs are connected only "**1st Drive**" and "**2nd Drive**" are listed.

The boot sequence can be selected from the available devices. If the "**1st Drive**" option is selected a list of available HDDs are shown. Select the first HDD you wish the system to boot from. If system does not boot from the "**1st Drive**" it may also disabled.

5.6.4 Removable Drives

The **Removable Drives** menu (**BIOS Menu 18**) specifies the boot sequence of the available removable drives. When the menu is opened, the removable drives connected to the system are listed as shown below:

- 1st Drive [Drive Details]
- 2nd Drive [Drive Details]

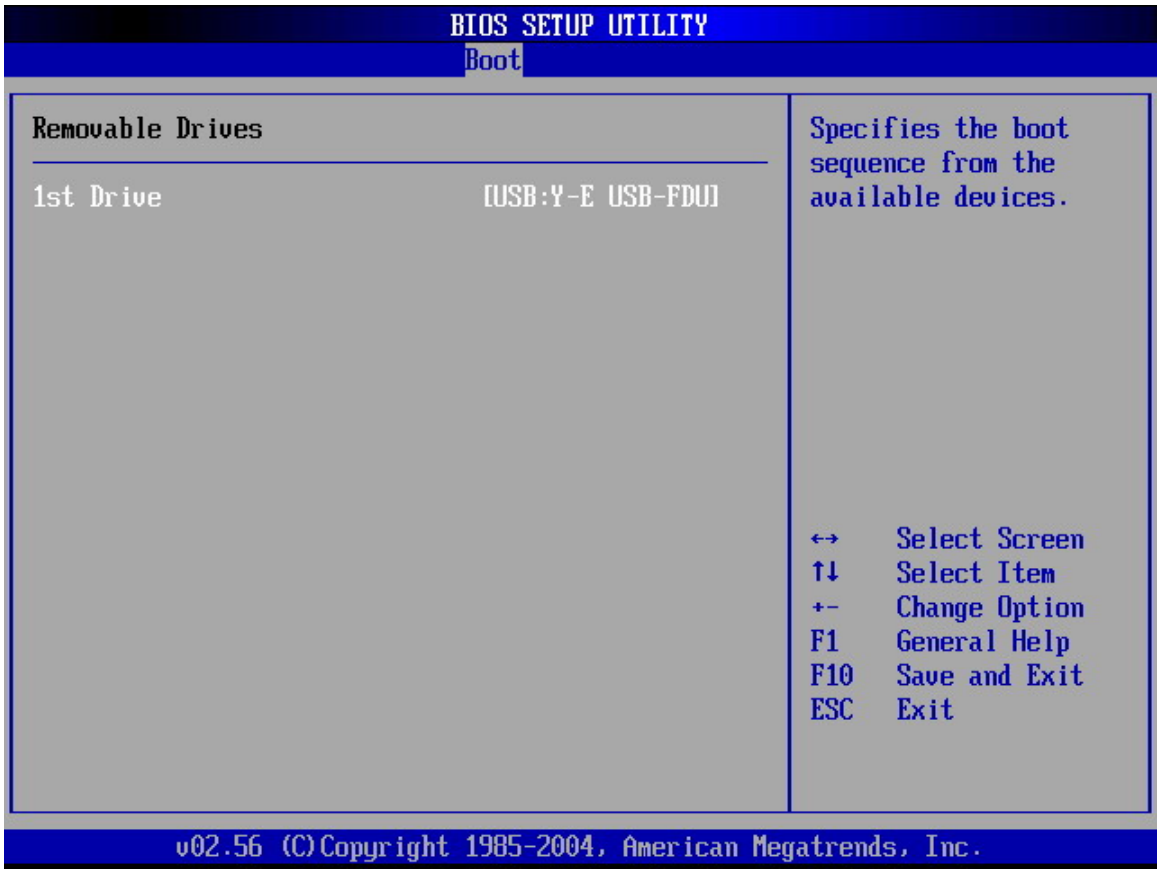
NOTE:

Only the drives connected to the system are shown. For example, if only one removable drive is connected only "**1st Drive**" is listed.

The boot sequence from the available devices is selected. If "**1st Drive**" option is selected a list of available removable drives are shown. Select the first removable drive the system is to boot from. If system does not boot from the "**1st Drive**" it may also disabled.

NOTE:

There is no floppy disk function on the CZGG LU-10-X. The removable drives that may be listed include USB drives.



BIOS Menu 18: Removable Drives

5.6.5 CD/DVD Drives

The CD/DVD Drives menu is similar to the **Removable Drives BIOS Menu 18** and it specifies the boot sequence of the available CD/DVD drives. When the menu is opened, the CD drives and DVD drives connected to the system are listed as shown below:

- 1st Drive [CD/DVD: PM-(part ID)]
- 2nd Drive [HDD: PS-(part ID)]
- 3rd Drive [HDD: SM-(part ID)]
- 4th Drive [HDD: SM-(part ID)]

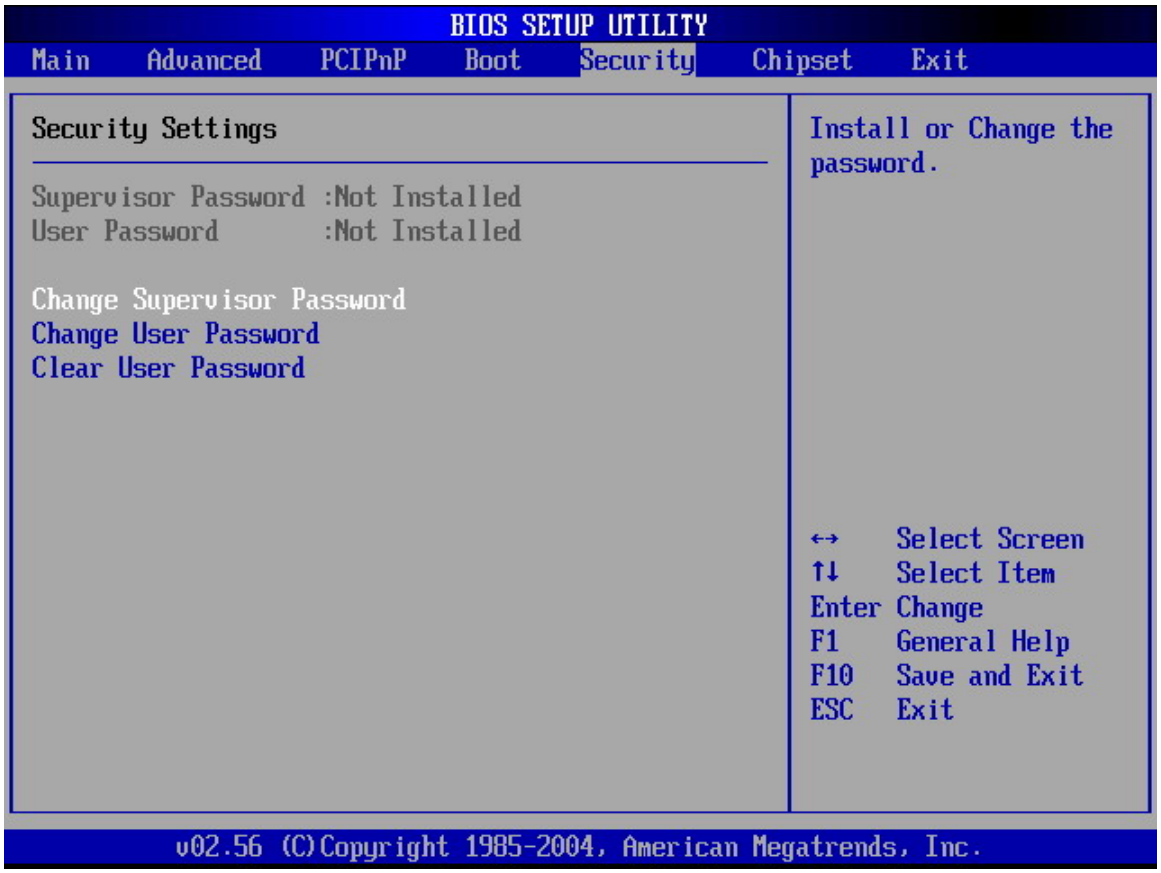
NOTE:

Only the drives connected to the system are shown. For example, if only two CDs or DVDs are connected only "**1st Drive**" and "**2nd Drive**" are listed.

Select the boot sequence from the available devices. If the "**1st Drive**" option is selected, a list of available HDDs are shown. Select the first HDD the system is to boot from. If system does not boot from the "**1st Drive**" it may also disabled.

5.7 Security

The **Security** menu (**BIOS Menu 19**) allows you to configure the system security settings including passwords.



BIOS Menu 19: Security

➔ **Change Supervisor Password**

The default setting for the **Change Supervisor Password** is **Not Installed**. If you wish to install a supervisor password, select this field and enter the password. After the password has been added, a **User Access Level** option and a **Password Check** option appear.

➔ **User Access Level [Full Access]**

The **User Access Level** option allows you to specify the access a normal user has to the BIOS settings.

➔	**No Access**		Users have no access to the Setup Utility
➔	**View Only**		Users can only view the Setup Utility
➔	**Limited**		Users can change limited fields like date and time
➔	**Full Access**	(Default)	Users have full access to the Setup Utility

➔ **Change User Password**

The default setting for the Change User Password is Not Installed. If you wish to install a user password, select this field and enter the password. After the password has been added, Install appears next to Change User Password.

➔ **Password Check [Setup]**

The **Password Check** option allows you to specify when a user is prompted for the password.

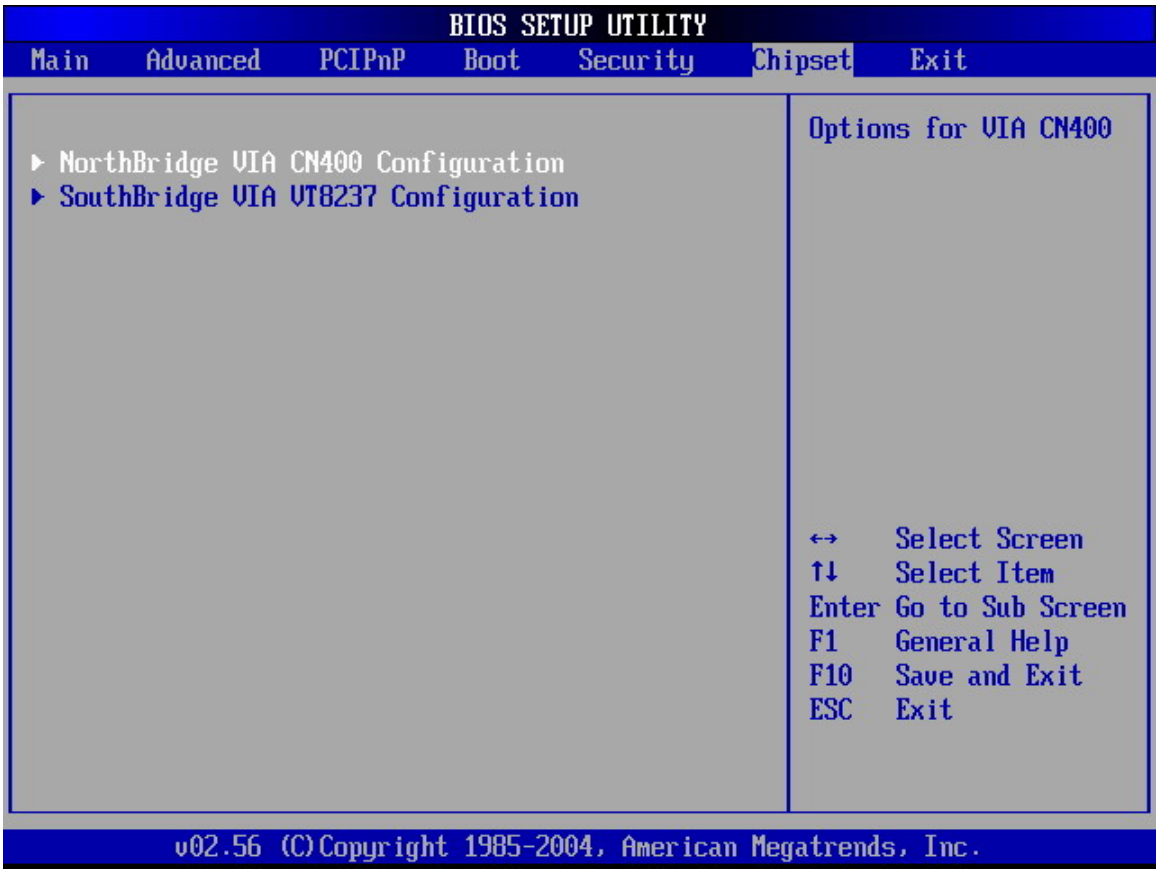
➔ **Setup**	(Default)	Users have to enter their password only when they enter the Setup Utility
➔ **Always**		Users have to enter their password whenever they boot the computer

5.8 Chipset

The **Chipset** menu (**BIOS Menu 20**) has two sub-menus, Northbridge VIA CN400 Configuration and Southbridge VIA VT8237 Configuration. The Northbridge submenu configures the Northbridge chipset and the Southbridge submenu configures the Southbridge chipset.

WARNING!

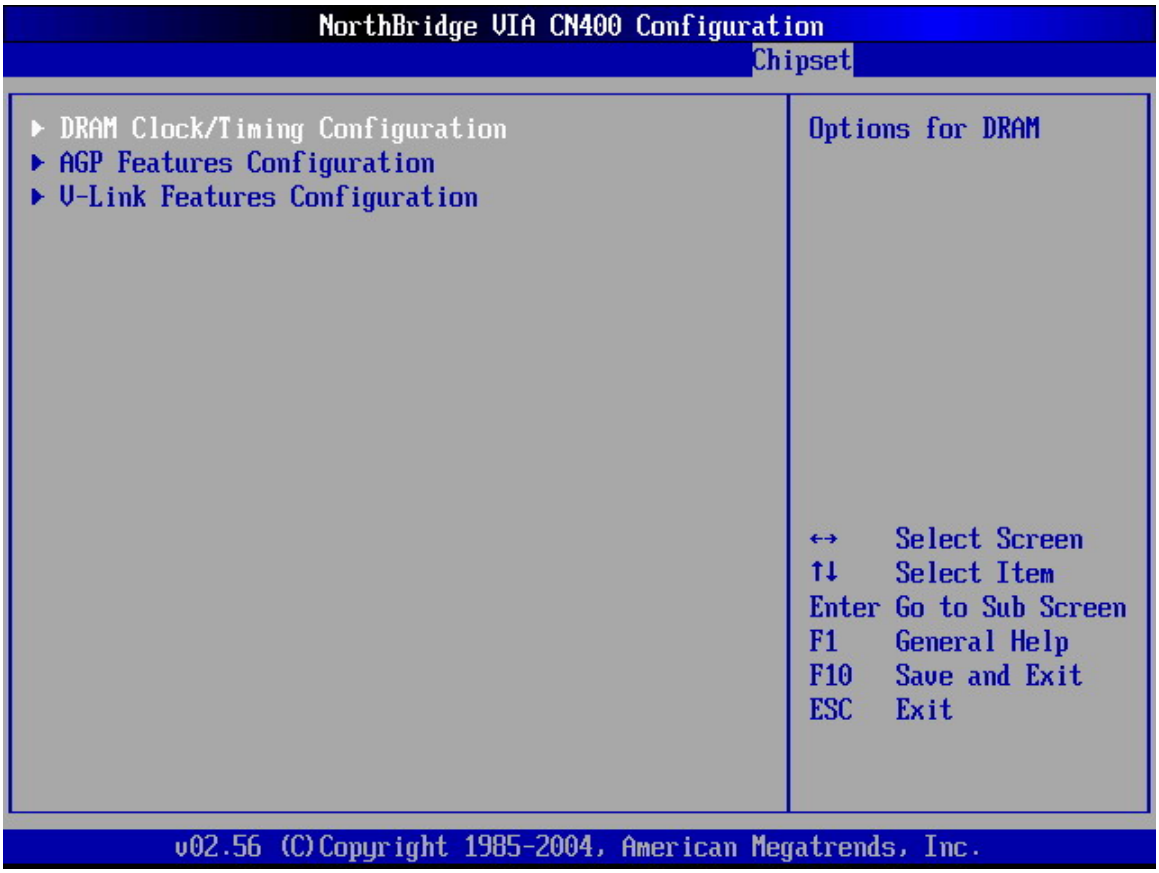
Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.



BIOS Menu 20: Chipset

5.8.1 Northbridge VIA CN400 Configuration

The Northbridge VIA CN400 Configuration menu (BIOS Menu 20) configures the Northbridge chipset.



BIOS Menu 21: Northbridge Chipset Configuration

The Northbridge VIA CN400 Configuration BIOS menu has three submenus

- DRAM Clock/Timing Configuration
- AFO Features Configuration
- V-LINK Features Configuration

The **Northbridge VIA CN400** Configuration BIOS menu has a single configurable option:

➔ **Top Performance [Disabled]**

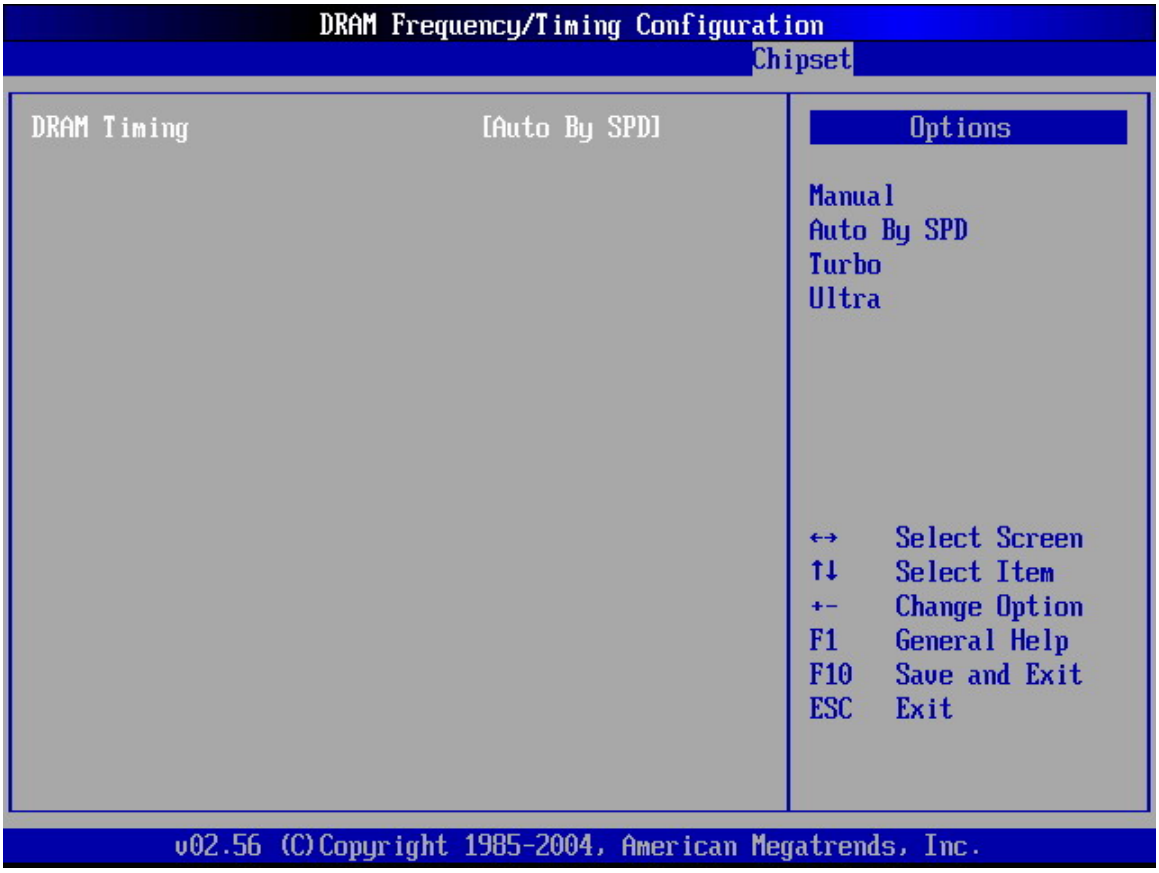
The **Top Performance** BIOS option has two configuration options:

➔ **Disabled** (Default)

➔ **Enabled**

5.8.1.1 DRAM Clock/Timing Configurations

The DRAM Clock/Timing Configuration menu (BIOS Menu 20) configures the DRAM settings.



BIOS Menu 22: DRAM Clock/Timing Configuration

➔ **DRAM Frequency [Auto]**

The **DRAM Frequency** option specifies the DRAM frequency or allows the system to automatically detect the DRAM frequency.

➔	**200MHz**		Sets the DRAM frequency to 200MHz
➔	**266MHz**		Sets the DRAM frequency to 266MHz
➔	**333MHz**		Sets the DRAM frequency to 333MHz
➔	**Auto**	(Default)	Automatically selects the DRAM frequency

➔ **DRAM Timing by SPD [Auto by SPD]**

The **Configure DRAM Timing by SPD** determines if the system uses the SPD *(*Serial Presence Detect) EEPROM to configure the DRAM timing. The SPD EEPROM contains all necessary DIMM specifications the including speed of the individual components such as CAS and bank cycle time as well as valid settings for the module and the manufacturer's code. The SPD enables the BIOS to read the spec sheet of the DIMMs on boot-up and then adjust the memory timing parameters accordingly.

➔	**Manual**		DRAM timing parameters can be manually set using the DRAM sub-items
➔	**Auto by SPD**	(Default)	DRAM timing parameter are set according to the DRAM Serial Presence Detect (SPD)

➔ **Turbo**

➔ **Ultra**

The **Configure DRAM Timing by SPD** option is disabled, the following configuration options appear.

- SDRAM CAS# Latency [2.5]
- SDRAM Bank Interleave [Disabled]
- Precharge to Active (Trp) [4T]
- Active to Precharge (Tras) [9T]
- Active to CMD (Trcd) [4T]
- REF to ACT/REF to REF(Trfc) [15T]
- ACT (0) ti ACT (1) (Trrd) [3T]

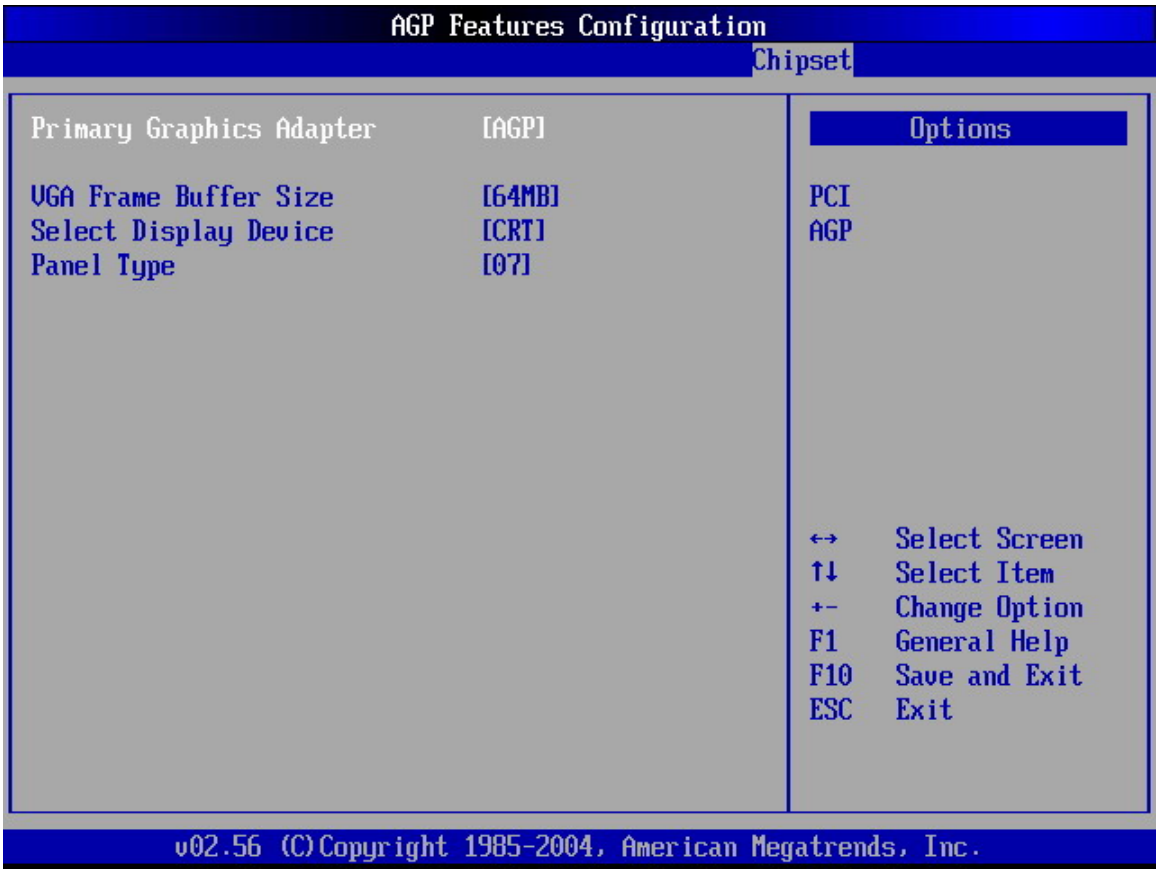
➔ **DRAM Command Rate [2T Command]**

➔ **2T Command** (Default)

➔ **1T Command**

5.8.1.2 AGP Features Configuration

The AGP Features Configuration menu (BIOS Menu 20) configures the AGP settings.



BIOS Menu 23: AGP Features Configuration

➔ **Primary Graphics Adapter [AGP]**

The **Primary Graphics Adapter** selects the graphics adapter the system uses.

➔ **PCI** (Default) PCI graphics adapter is used

➔ **AGP** AGP graphics adapter is used

➔ **VGA Frame Buffer Size [64MB]**

The **VGA Frame Buffer** Size BIOS option sets the memory buffer size for the VGA display. The following buffer sizes can be set:

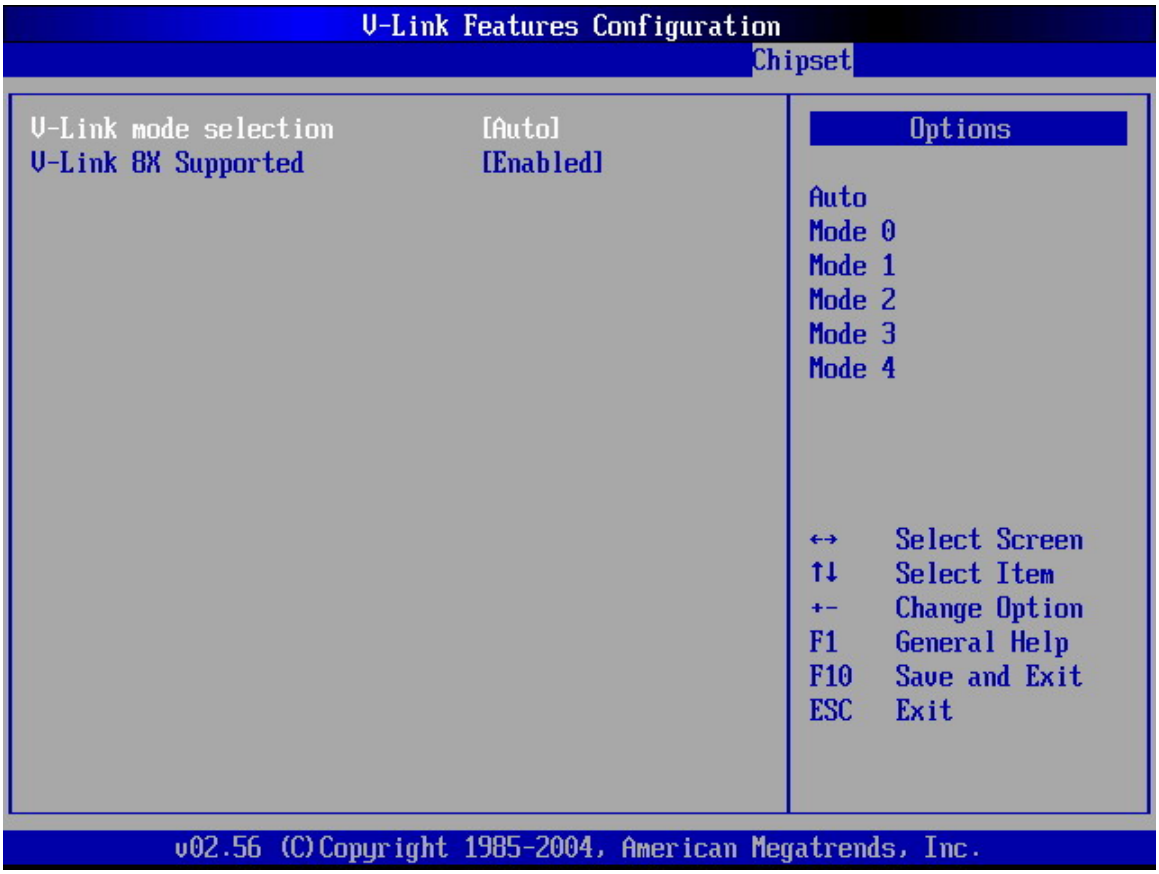
- None
- 8MB
- 16MB
- 32MB
- 64MB

➔ **Panel Type [07]**

The **Panel Type** option specifies the device the panel type. The user is prompted to enter number between 0 and 15.

5.8.1.3 V-Link Features Configuration

The V-Link Features Configuration menu (**BIOS Menu 20**) configures the V-Link Features.



BIOS Menu 24: V-Link Configuration

➔ **V-Link Mode Selection [Auto]**

The **V-Link Mode Selection** controls V-Link bus operation. The following options are available.

- Auto
- Mode 0
- Mode 1
- Mode 2
- Mode 3

- Mode 4

➔ **V-Link Data 8X Supported [Disabled]**

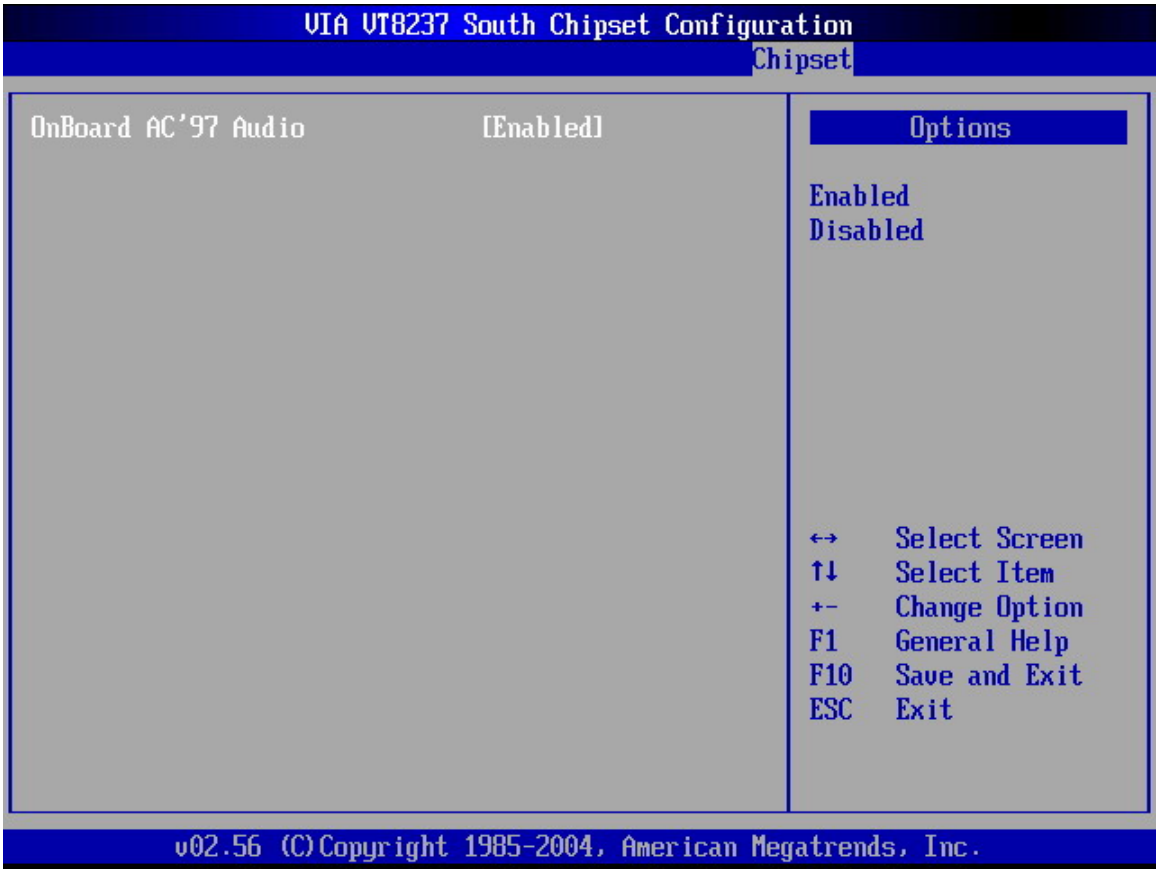
The **V-Link Data 8X Support** controls the data transmission speed between the Northbridge and Southbridge chipsets.

➔ **Disabled** V-LINK Data 8x transmissions not supported and the transmission speed between the integrated Northbridge and Southbridge decreases.

➔ **Enabled** (Default) V-LINK Data 8x transmissions supported and the transmission speed between the integrated Northbridge and Southbridge increases.

5.8.2 SouthBridge Configuration

The SouthBridge Configuration menu (BIOS Menu 25) configures the southbridge chipset.



BIOS Menu 25:SouthBridge Chipset Configuration

➔ **OnBoard AC'97 [Enabled]**

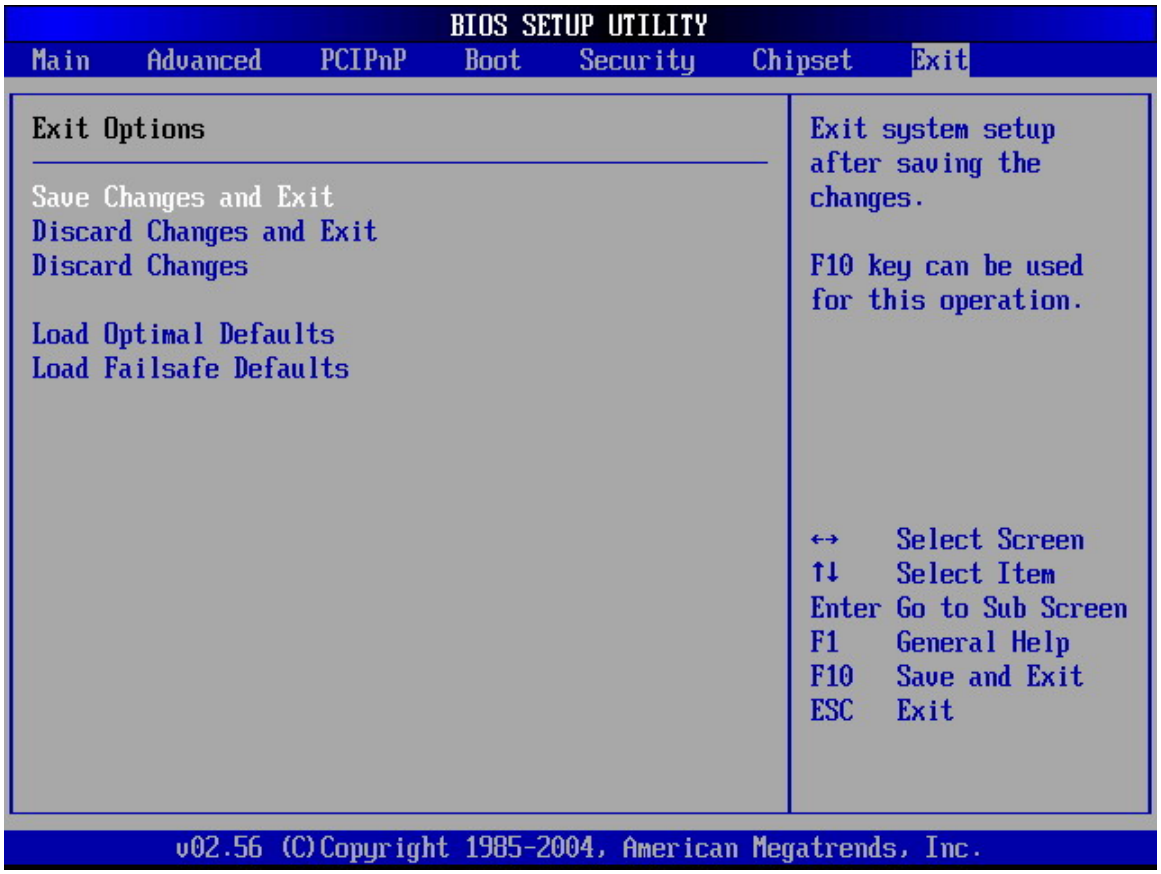
The **OnBoard AC97 Audio** enables or disables the AC'97 CODEC.

➔ **Disabled** The onboard AC'97 is disabled

➔ **Enabled** (Default) The onboard AC'97 automatically detected and enabled

5.9 Exit

The **Exit** menu (**BIOS Menu 26**) allows default BIOS values to be loaded, optimal failsafe values and to save configuration changes.



BIOS Menu 26: Exit

➔ **Save Changes and Exit**

If configuration changes are complete and a user wishes to save them and exit the BIOS menus, select this option.

➔ **Discard Changes and Exit**

If you have finished making configuration changes but do not want to save them and you want to exit the BIOS menus, select this option.

➔ **Discard Changes**

If you have finished making configuration changes but do not want to save them but still want to continue working with BIOS, select this option.

➔ **Load Optimal Defaults**

This option allows you to load optimal default values for each of the parameters on the Setup menus. F9 key can be used for this operation.

➔ **Load Failsafe Defaults**

This option allows you to load failsafe default values for each of the parameters on the Setup menus. F8 key can be used for this operation.

Intentionally Blank

Chapter

6

Software Drivers

6.1 Available Software Drivers

NOTE:

The contents of the CD may vary throughout the life cycle of the product and is subject to change without prior notice. Visit www.cyberresearch.com or contact technical support for the latest updates.

The CZGG LU-10-X board has three software drivers:

- Chipset
- Audio
- LAN

All three drivers can be found on the CD that came with the CZGG LU-10-X. To install the drivers please follow the instructions in the sections below:

6.2 Chipset Driver Installation

To install the chipset driver, please follow the steps below:

Step 1: Insert the CD into the system that contains the CZGG LU-10-X board.

Step 2: Open the "**VIA**" folder. Open the "**4in1 Extreme**" subfolder. (See **Figure 6-1**)

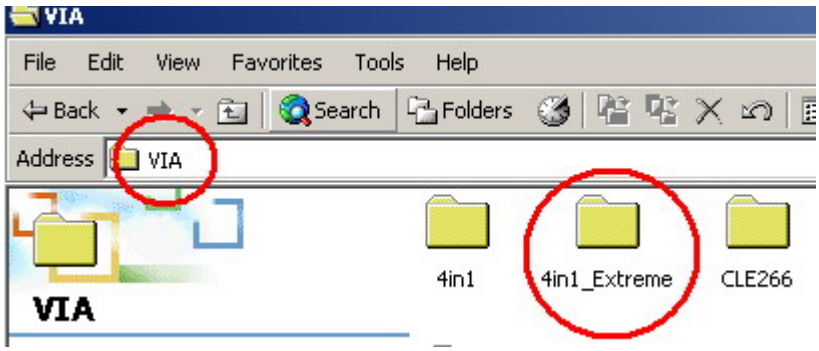


Figure 6-1: Access the 4in1_Extreme Folder

Step 3: Click the Setup utility icon shown in **Figure 6-2**.

Figure 6-2: Setup Utility Icon

Step 4: The installation program begins to initialize. After the initialization process a welcome screen shown in **Figure 6-3** appears. Click "**NEXT**" to continue the installation.

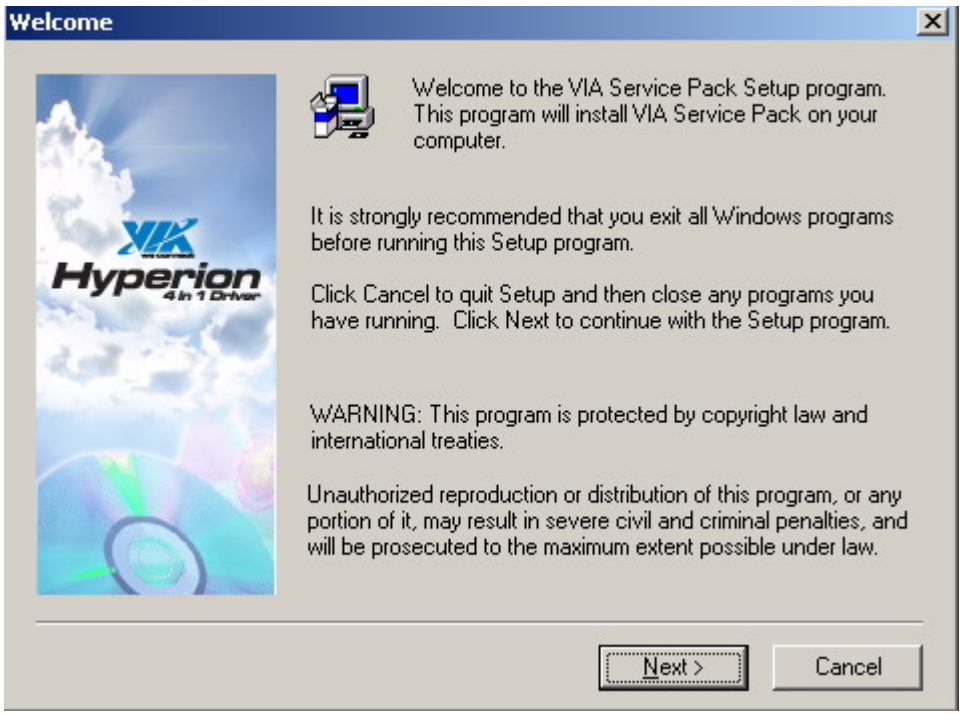


Figure 6-3: VIA Chipset Driver Installation Welcome Screen

Step 5: The "**Readme**" in **Figure 6-4** appears. Click "**NEXT**" to continue the installation.

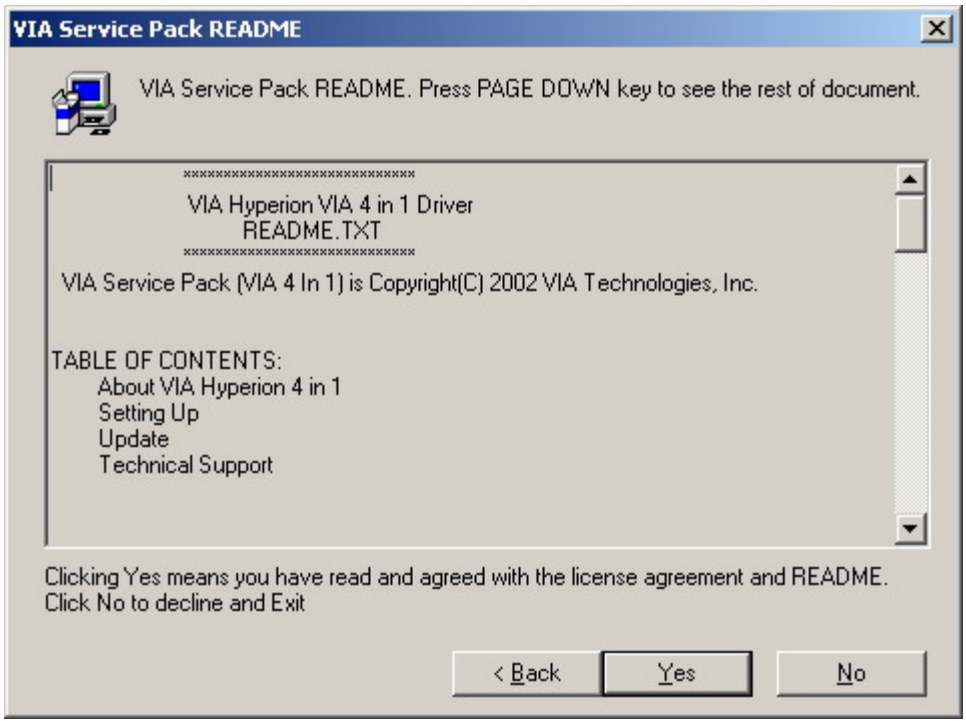


Figure 6-4: Readme Information

Step 6: The user is then prompted to select the installation type. A user can select "**Normal Installation**" or "**Quick Installation**." (See **Figure 6-5**) Select the installation type and click "**NEXT**" to continue the installation.

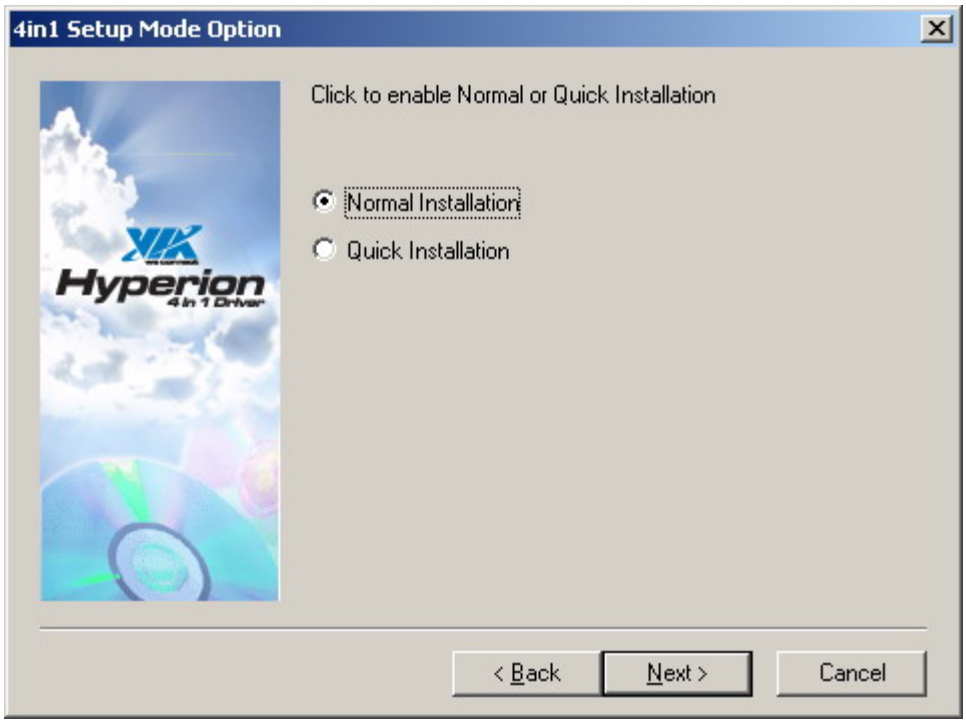


Figure 6-5: VIA Chipset Driver Installation Type

Step 7: The setup then prompts the user (see **Figure 6-6**) to select the drivers that must be installed on the system. There are three drivers:

- VIA PCI IDE Bus Driver
- AGP Driver (AGP3.0 Supported)
- VIA INF Driver 2.20A

Select the drivers that must be installed on the system. Click "**NEXT**" to continue the installation.

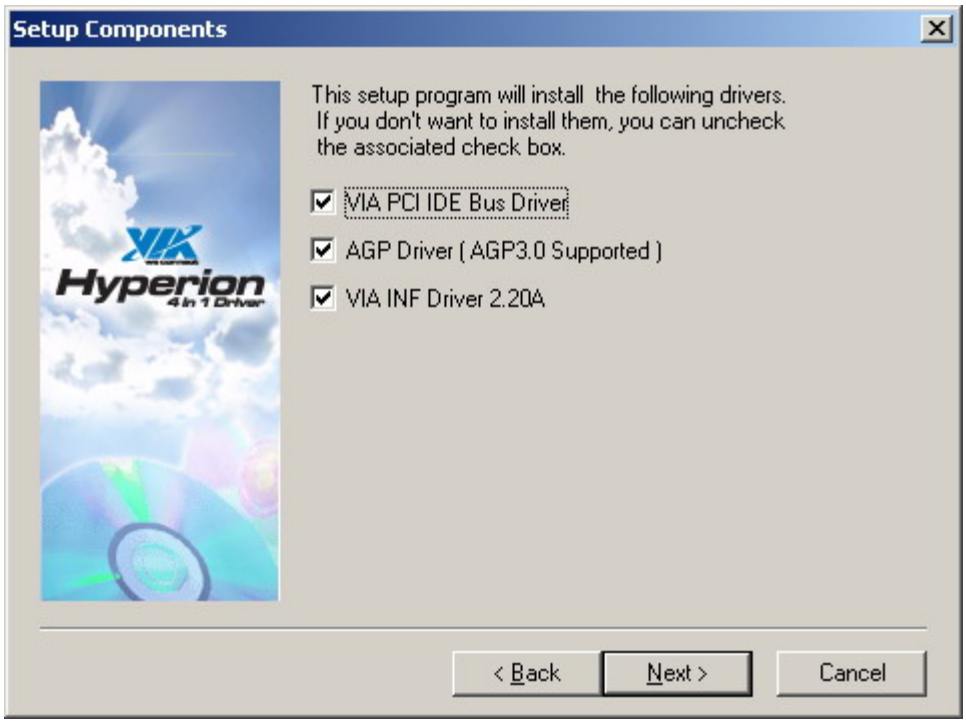


Figure 6-6: Driver Selection

Step 8: The setup then prompts the user (see **Figure 6-7**) if the VIA PCI IDE Bus Driver must be installed on the system. Select install or uninstall. Click "**NEXT**" to continue the installation.

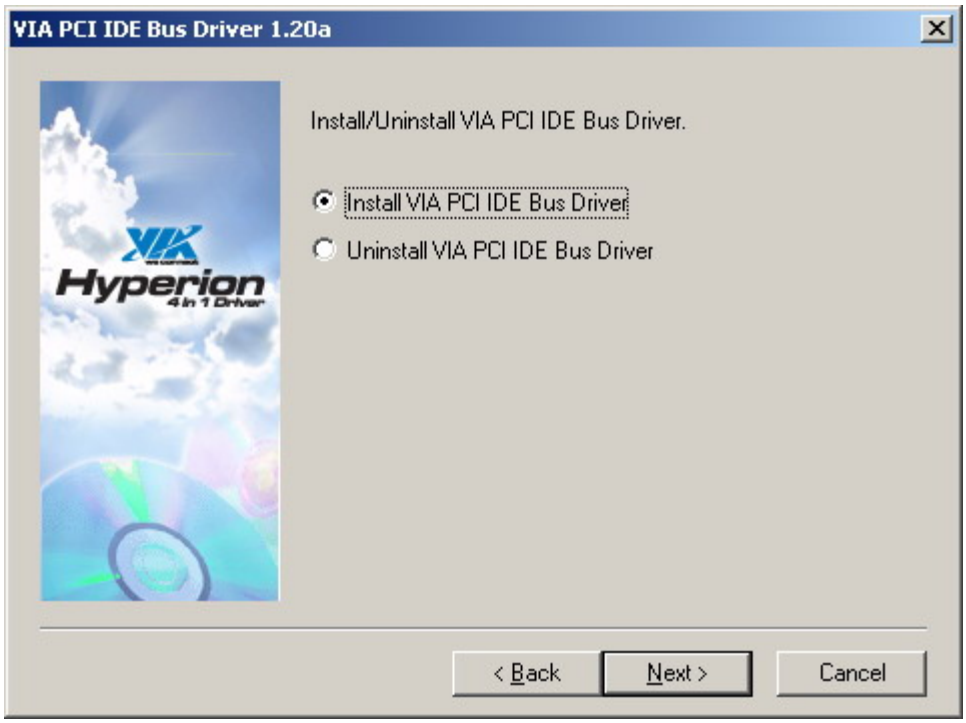


Figure 6-7: VIA PCI IDE Bus Driver Selection

Step 9: The drivers are then installed onto the system. After the installation is complete the user is prompted to restart the computer now or later. (See **Figure 6-8**) Select when the computer must be restarted. Click "**OK**" to exit the installation program.

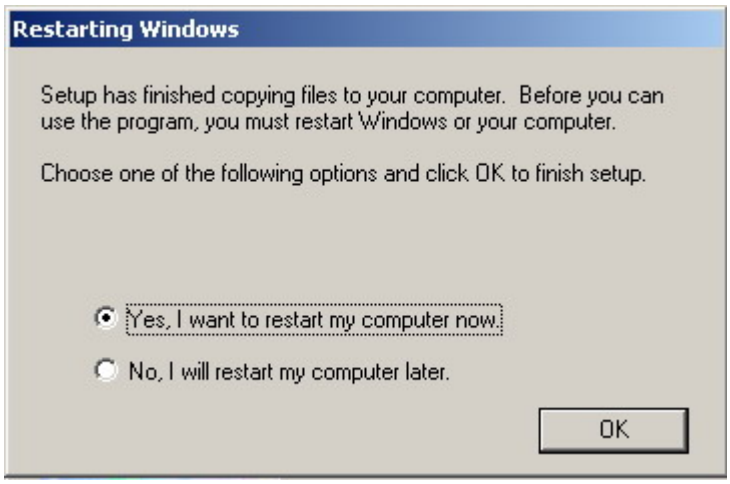


Figure 6-8: Restart the Computer

6.3 RealTek Audio Driver Installation

To install the RealTek AC'97 Audio driver, please follow the steps below:

Step 1: Insert the CD into the system that contains the CZGG LU-10-X board. Open the CD folder and locate the **AUDIO DRIVER A3.79** directory. Open the directory and look for icon for the **setup.exe** installation file. Once located, use the mouse to move the cursor over the icon and double click the mouse button.

Step 2: Once the double click the **Setup** icon is clicked, the install shield wizard for the audio driver starts. See **Figure 6-9.**

Figure 6-9: Audio Driver Install Shield Wizard Starting

Step 3: The RealTek Audio Setup prepares the install shield to guide you through the rest of the setup process. See **Figure 6-10**.

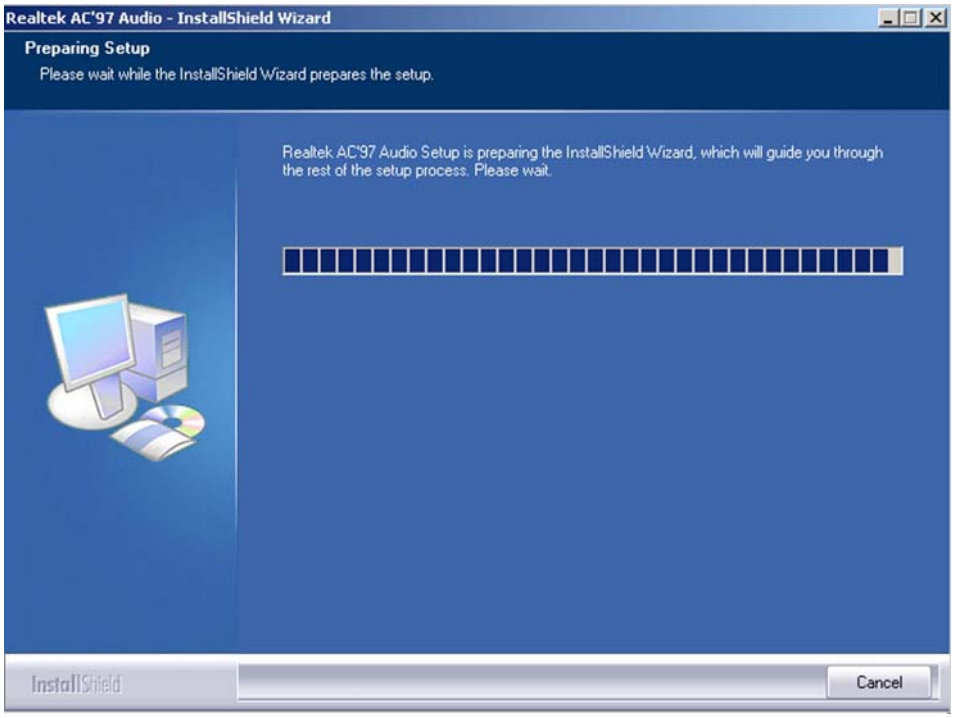


Figure 6-10: Audio Driver Setup Preparation

Step 4: After install shield is prepared, the welcome screen shown in **Figure 6-11** appears. To continue the installation process, click the "**NEXT**" button. The install shield starts to configure the new software as shown in **Figure 6-12**.

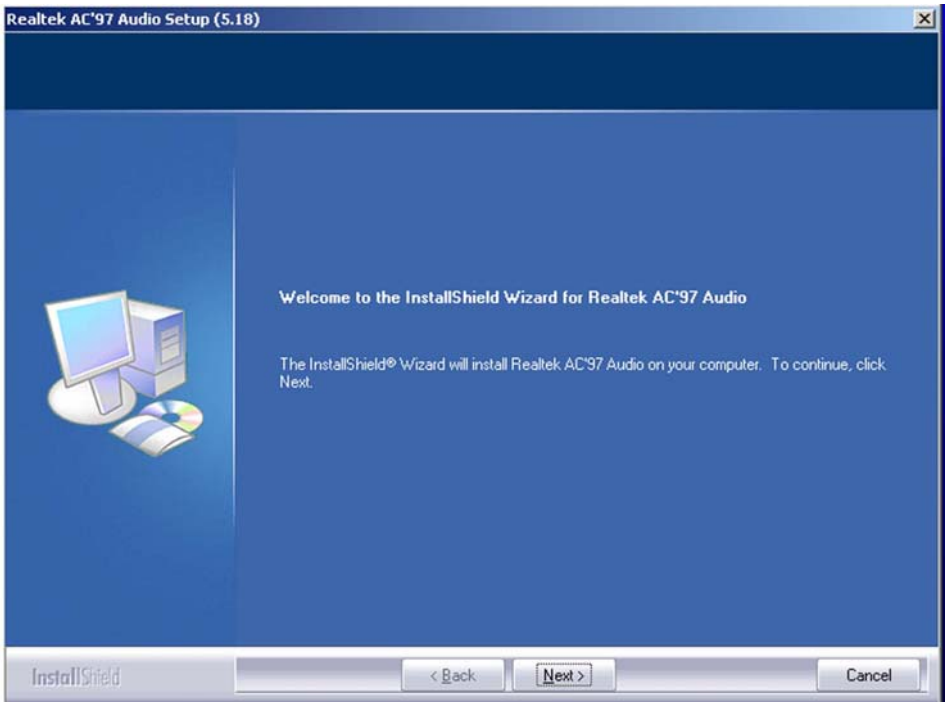


Figure 6-11: Audio Driver Welcome Screen

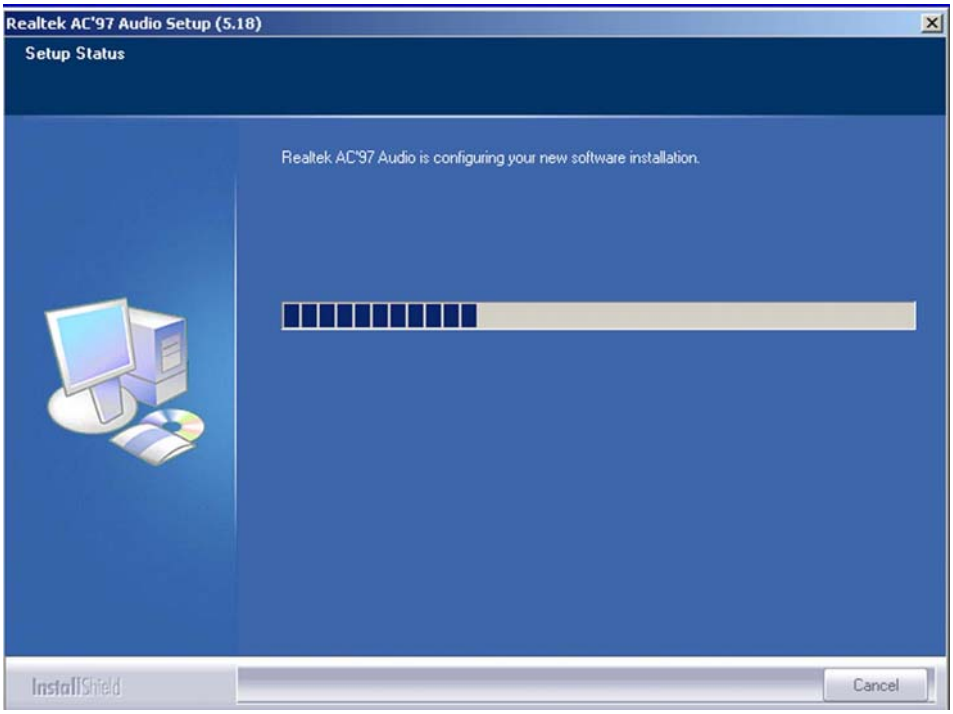


Figure 6-12: Audio Driver Software Configuration

Step 5: At this stage the "**Digital Signal Not Found**" screen shown in **Figure 6-13**

appears. To continue the installation process, click the "**YES**" button. The installation notice shown below appears.

Figure 6-13: Audio Driver Digital Signal

Step 6: At this stage the clicking the "**YES**" button in **Figure 6-13** appears, the installation of the driver begins. See **Figure 6-14**.

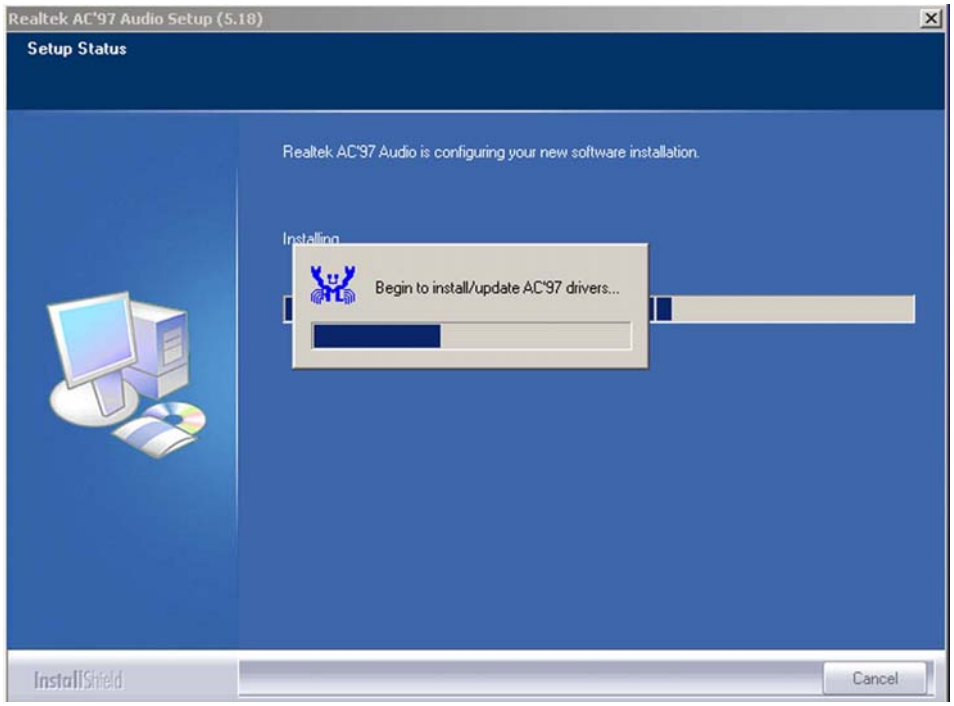


Figure 6-14: Audio Driver Installation Begins

Step 7: After the driver installation process is complete, a confirmation screen shown in **Figure 6-15** appears

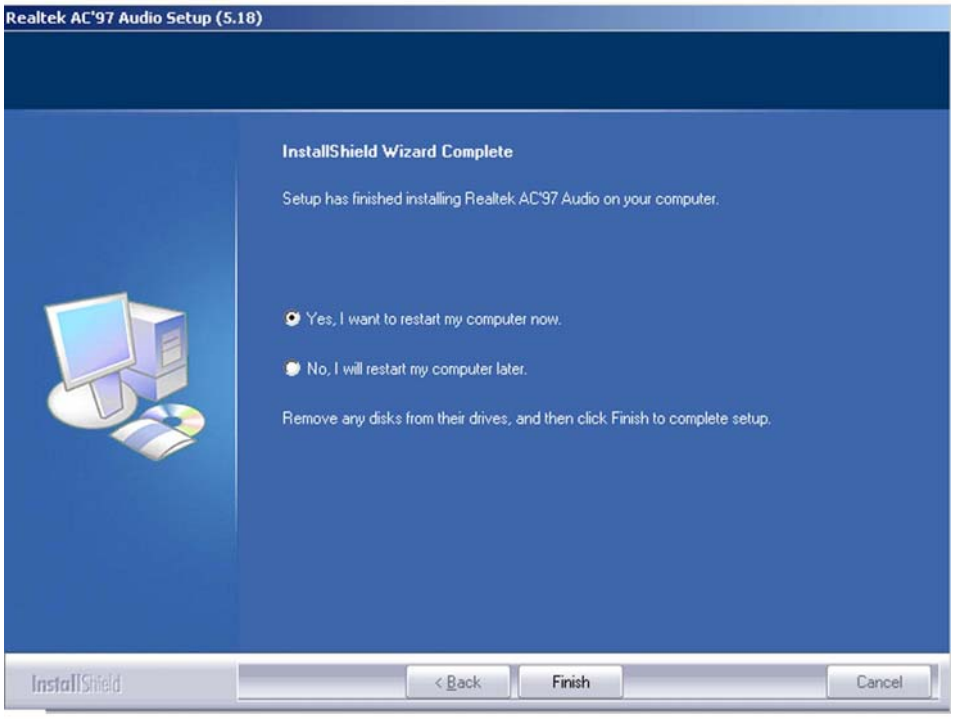


Figure 6-15: Audio Driver Installation Complete

Step 8: The confirmation screen shown in **Figure 6-15** allows you to restart the computer immediately after the installation is complete or to restart the computer later. For the settings to take effect the computer must be restarted. Once you have decided when to restart the computer, click the "**FINISH**" button.

6.4 LAN Driver Installation

To install the LAN driver, please follow the steps below:

Step 1: Insert the CD into the system that contains the CZGG LU-10-X. Open the **LAN** directory and locate the icon for the relevant **Setup** installation file. Once located, use the mouse to move the cursor over the icon and double click the mouse button.

Step 2: Once you double click the **Setup** icon, a **LAN License Agreement** screen shown in **Figure 6-17** appears.

Figure 6-16: LAN License Agreement

Step 3: If you accept the terms, click "**Next**." You are then prompted for the directory the driver is stored in. (See **Figure 6-17**)

Figure 6-17: Select the Driver Directory

Step 4: After selecting the directory the driver is installed in, click "**Next**." The screen in **Figure 6-18** appears.

Figure 6-18: LAN Driver Configuration

Step 5: In **Figure 6-18** you have three options.

- Install Base Driver → Installs the base driver
- Make Driver Disk → Copies the driver to disk
- View Release Notes → Opens word document of the release notes

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Appendix

A

BIOS Configuration Options

A.1 BIOS Configuration Options

Below is a list of BIOS configuration options described in **Chapter 5**.

Appendix

B

Watchdog Timer

NOTE:

The following discussion applies to the DOS environment. It is recommended you contact CyberResearch support or visit our website for specific drivers for other operating systems.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMI or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer:

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer's period.
BL:	Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup).

Table B-1: AH-6FH Sub-function

You have to call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. While the timer value reaches zero, the system will reset. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the Watchdog timer will be disabled if you set the time-out value to be zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

NOTE:

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system will reset.

Example program:

```
; INITIAL TIMER PERIOD COUNTER
;
W_LOOP:

        MOV     AX, 6F02H       ;setting the time-out value
        MOV     BL, 30          ;time-out value is 48 seconds
        INT      15H
 ;
; ADD YOUR APPLICATION PROGRAM HERE
;
        CMP      EXIT_AP, 1     ;is your application over?
        JNE      W_LOOP         ;No, restart your application

        MOV     AX, 6F02H       ;disable Watchdog Timer
        MOV     BL, 0           ;
        INT      15H
;
; EXIT ;
```


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Appendix

C

Address Mapping

C.1 IO Address Map

I/O address Range	Description
000-01F	DMA Controller
020-021	Interrupt Controller
040-043	System time
060-06F	Keyboard Controller
070-07F	System CMOS/Real time Clock
080-09F	DMA Controller
0A0-0A1	Interrupt Controller
0C0-0DF	DMA Controller
0F0-0FF	Numeric data processor
1F0-1F7	Primary IDE Channel
2F8-2FF	Serial Port 2 (COM2)
378-37F	Parallel Printer Port 1 (LPT1)
3B0-3BB	VIA Graphics Controller
3C0-3DF	VIA Graphics Controller
3F6-3F6	Primary IDE Channel
3F7-3F7	Standard floppy disk controller
3F8-3FF	Serial Port 1 (COM1)

Table C-1: IO Address Map

C.2 1st MB Memory Address Map

Memory address	Description
00000-9FFFF	System memory
A0000-BFFFF	VGA buffer
F0000-FFFFF	System BIOS
1000000-	Extend BIOS

Table C-2: 1st MB Memory Address Map

C.3 IRQ Mapping Table

IRQ0	System Timer	IRQ8	RTC clock
IRQ1	Keyboard	IRQ9	ACPI
IRQ2	Available	IRQ10	LAN
IRQ3	COM2	IRQ11	LAN/USB2.0/SATA
IRQ4	COM1	IRQ12	PS/2 mouse
IRQ5	SMBus Controller	IRQ13	FPU
IRQ6	FDC	IRQ14	Primary IDE
IRQ7	Available	IRQ15	Secondary IDE

Table C-3: IRQ Mapping Table

C.4 DMA Channel Assignments

Channel	Function
0	Available
1	Available
2	Floppy disk (8-bit transfer)
3	Available
4	Cascade for DMA controller 1
5	Available
6	Available
7	Available

Table C-4: IRQ Mapping Table

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Appendix

D

External AC'97 Audio CODEC

D.1 Introduction

The audio functionalities of the CZGG LU-10-X CPU card can be implemented using a separately purchased audio module, contact CyberResearch, Inc for further details. The audio kit is powered by a Realtek ALC655 is a 16-bit, full duplex AC'97 2.3 compatible audio CODEC with 48KHz sampling rate. The audio kit's functionality is interfaced through three (3) phone jack connectors and two (2) pin headers including:

- A LINE input shared with surround output
- A MIC input shared with Center and LFE output
- A LINE output
- Analog line-level stereo inputs with 5-bit volume control: CDIN1 and AUXIN1.

Both Front_out and Surround_out are equipped with a built-in 50mW/20ohm amplifier. The ALC655 supports host/soft audio from Intel ICHx chipsets as well as audio controller based VIA/SIS/Ali/ATI chipset with bundled Windows series drivers (XP/ME/2000/98/NT), EAX/Direct Sound 3D/I3DL2/A3D compatible sound effect utilities supporting Karaoke, 26 kinds of environment sound emulations with 10-band equalizer, and HRTF 3D positional audio. The audio kit provides an excellent entertainment package sufficient for today's multimedia systems.

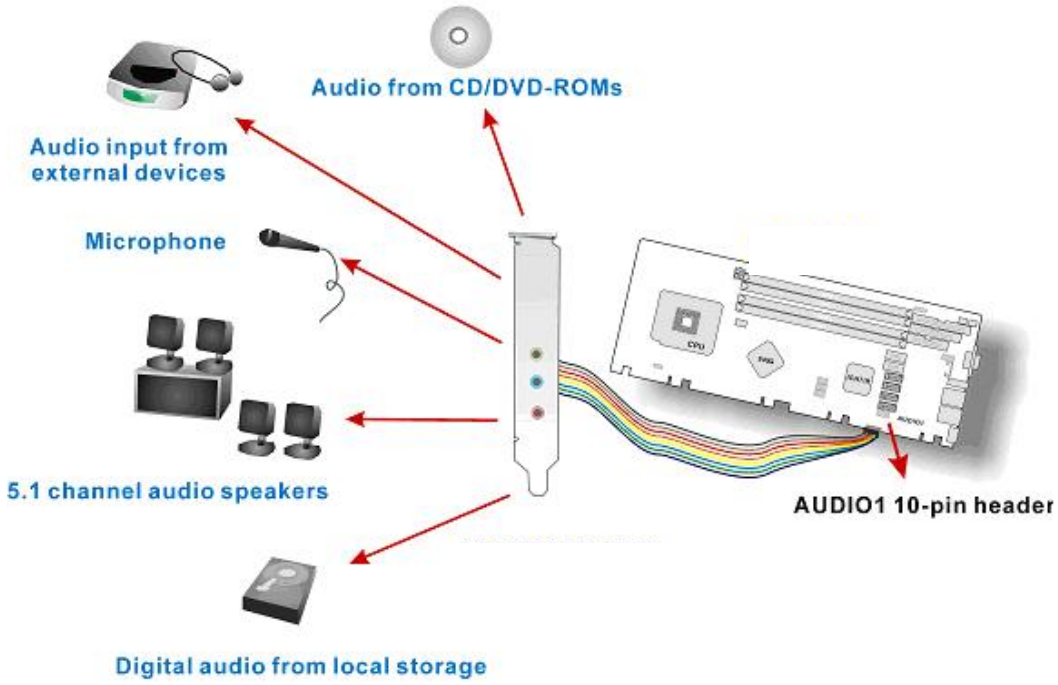

Figure D-1: Audio Functionalities via the Audio Kit

D.2 Physical Connection

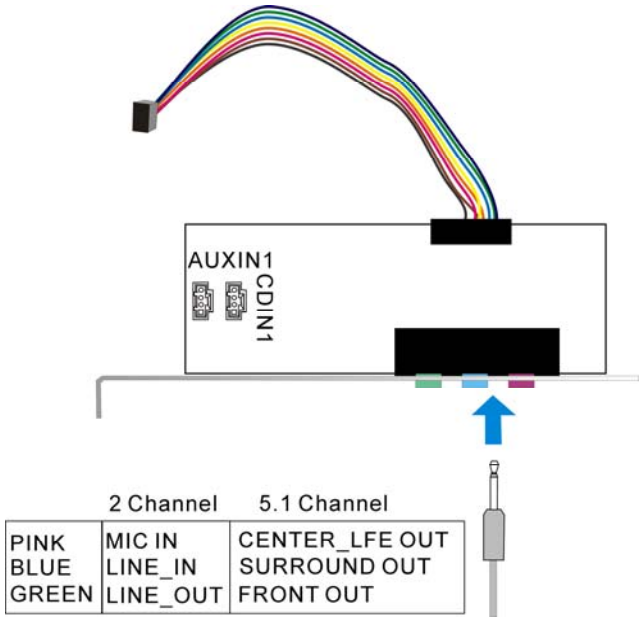

Figure D-2: Audio Kit Connectors

The audio kit comes with a PCI slot bracket for the installation into a PC case or rackmount chassis. Connect the 10-pin header to the AUDIO1 header as shown in Figure E-1, and if necessary, connect the CDIN1 and AUXIN1 to optical drives or other audio sources, e.g., an MPEG card, using a 4-pin cable. Note that depending on the devices you connect to, the phone jacks have different functions with different audio installation modes (2 channel or 5.1 channel modes).

D.3 Driver Installation

The driver installation has been described in Chapter 6, Section Step 7:.

After reboot, you should be able to find the sound effect configuration utility in Windows Control Panel (see **Figure D-3**); and if peripheral speakers have been properly connected, hear the sound effects.

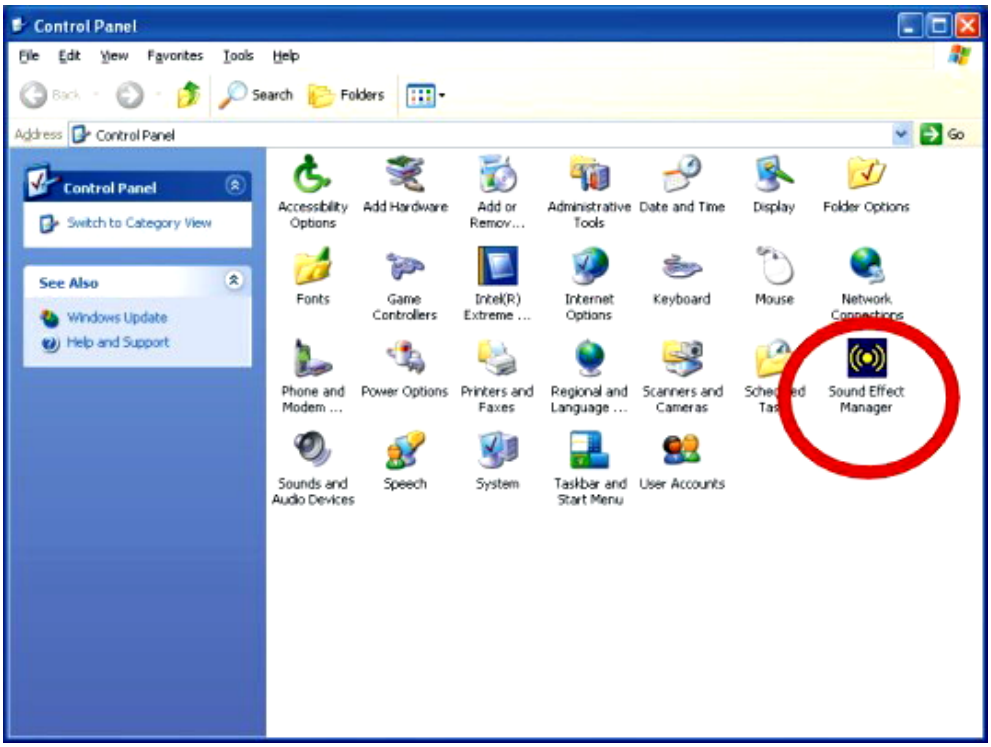

Figure D-3: Sound Effect Manager Icon

D.4 Sound Effect Configuration

After installing the audio CODEC driver, you should be able to use the multi-channel audio features. Click the audio icon from the Notification Area from system task bar (see **Figure D-5**). The shortcut to the configuration utility is also available through the **Sound Effect Manager** icon in the **Control Panel** (**Figure D-4**).

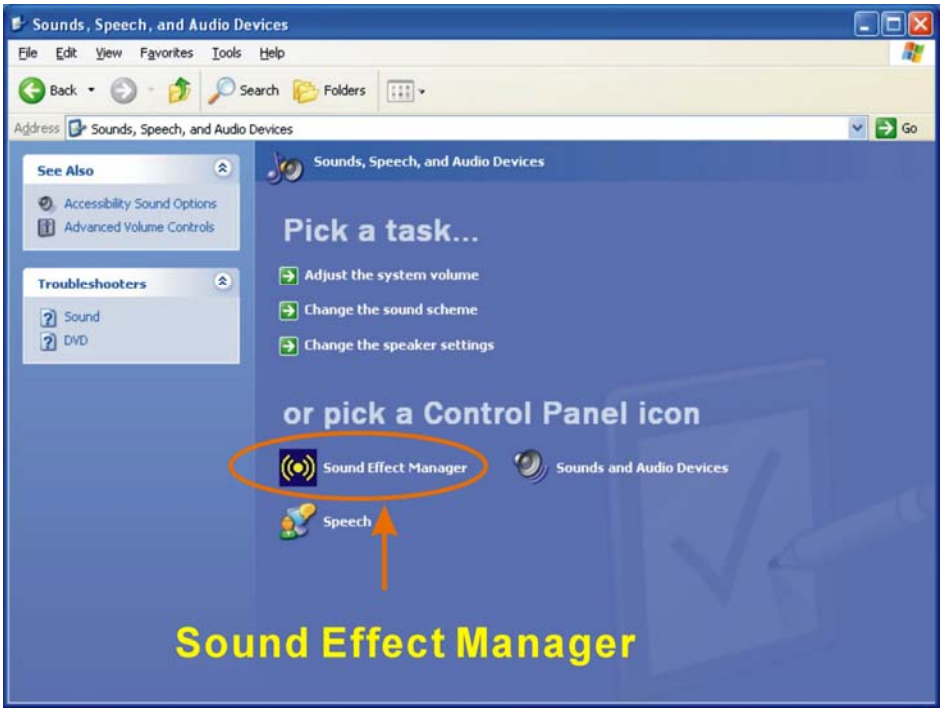

Figure D-4: Sound Effect Manager Icon [Control Panel]

Figure D-5: Sound Effect Manager Icon [Task Bar]

D.5 Sound Effect

You may select a pre-configured sound environment setting with the preset equalizer settings. You may also load an equalizer setting or make a new equalizer setting using the "**Load EQ Setting**" and "**Save Preset**" button. (See **Figure D-7**)

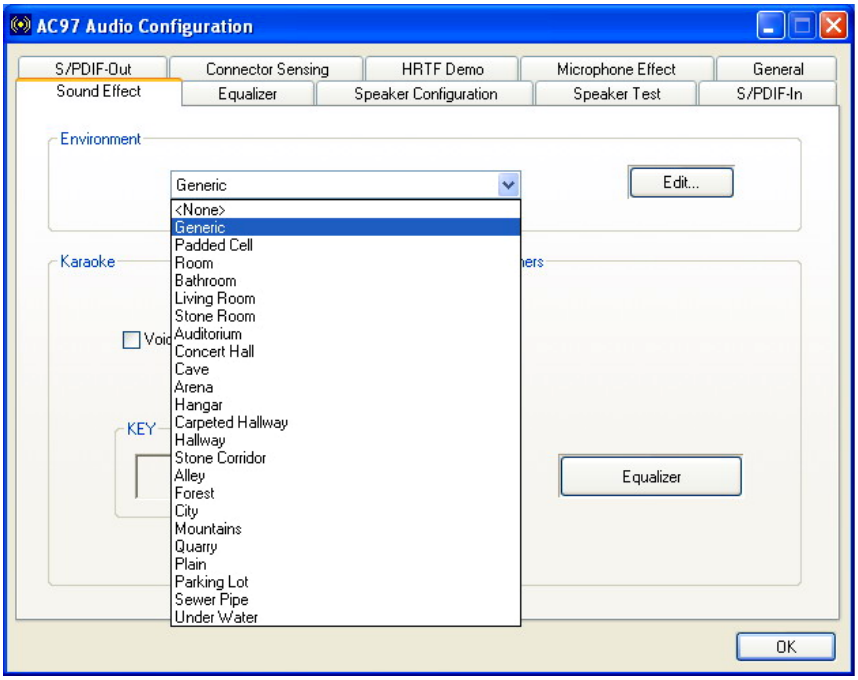

Figure D-6: Setting Sound Effects

D.6 Environment Simulation

This is the default screen whenever the configuration utility is opened.

You may select different sound environment modes by a single click on the Environment pull-down list. There are a total of 23 preset environment modes (see **Figure D-7**). You may also fine-tune the environment setting by clicking the **Edit** button on the right, which displays an editor window. Select a preset mode you want to edit. Then select one the property value from the list below with a single click. Use the scroll bar below to adjust properties setting. When you're done making adjustments, click the Save button.

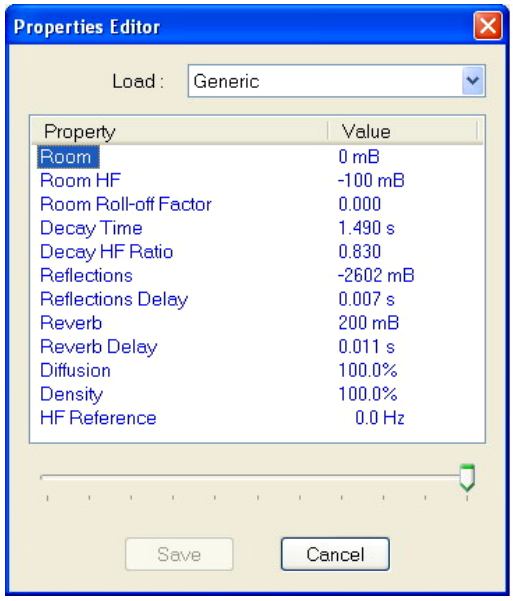

Figure D-7: Sound Effects Properties Editor

D.7 Karaoke Mode

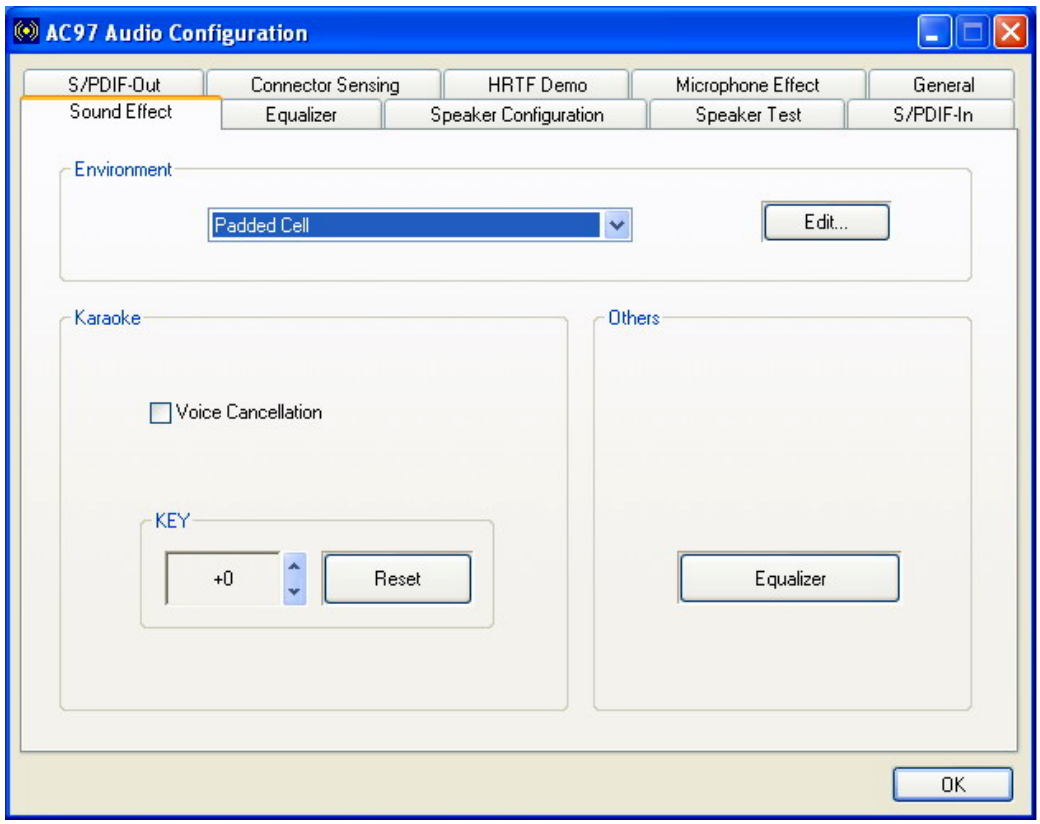

Figure D-8: Karaoke Mode

The Karaoke mode shown in **Figure D-8** allows you to eliminate the vocal of the music you play or adjust the key to accommodate your range.

The configuration options that come with the Karaoke function include:

Voice Cancellation: This checkbox, when selected, disables the vocal part of the music your play in your computer while the background music remains.

Key adjustment: Use the Up or Down arrow icons to find a key that fits your vocal range.

NOTE:

The Equalizer button on the default display brings you to the same configuration window as the Equalizer function tab on top of the window.

D.8 Equalizer Selection

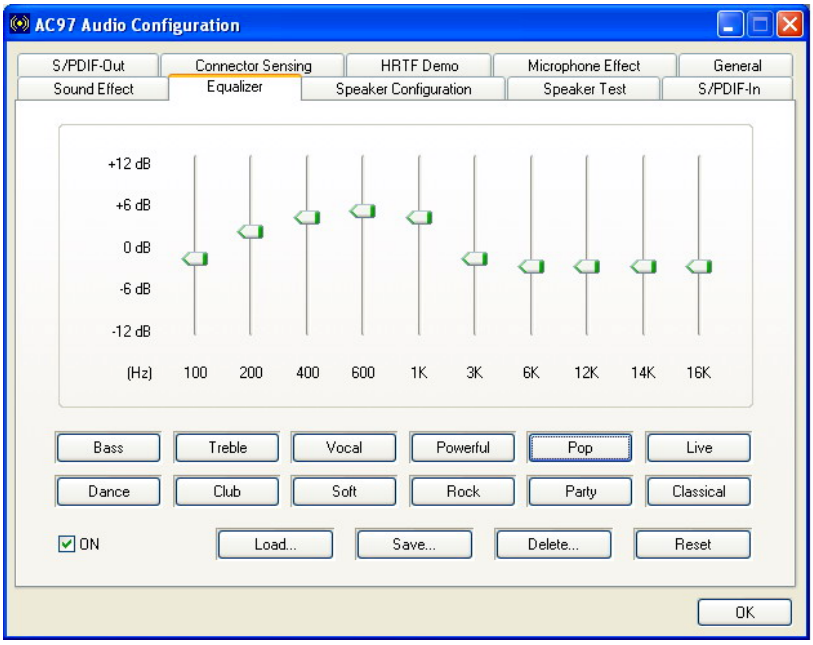

Figure D-9: Equalizer Settings

The equalizer in **Figure D-9** allows users to change sound effect parameters. The default screen shows equalized values. You may also select preset modes from the buttons below. The configurable values include 10 bands of equalizer ranging from 100Hz to 16KHz. Use the scroll bar to fine-tune, and use the **Load**, **Save**, **Delete**, and **Reset** buttons to edit your settings.

D.9 Speaker Configuration

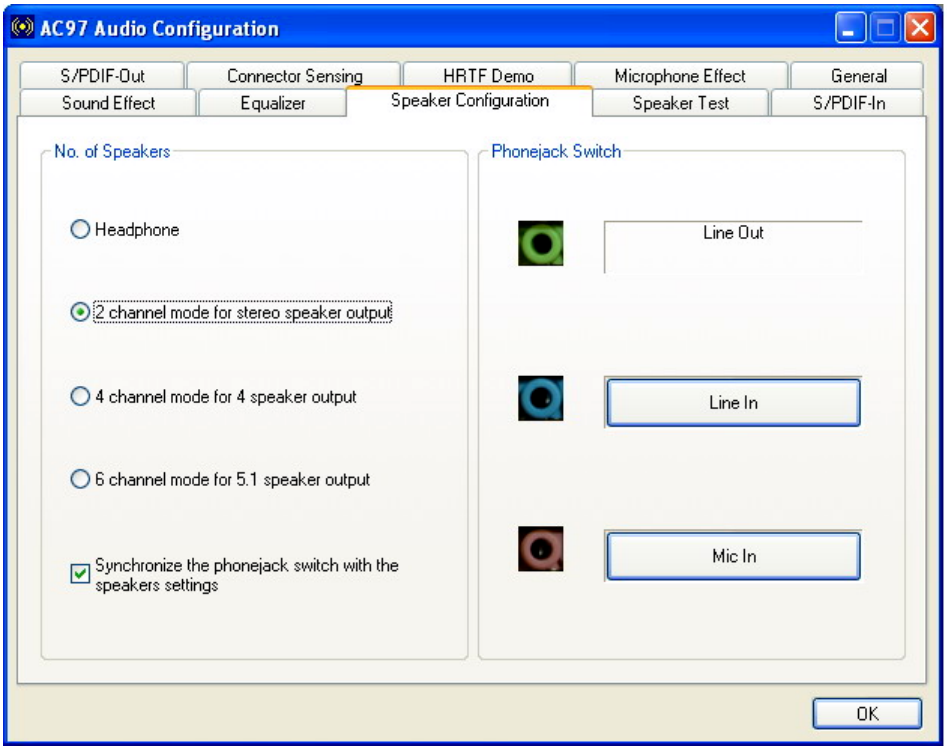

Figure D-10: Speaker Configuration

In this functional window, you can configure your multi-channel speaker settings.

Select the audio configuration from the **No. of Speakers** section on the left by clicking on one of the check circles.

The configurable options are:

- Headphone
- Channel mode for stereo speaker output
- Channel mode for 4 speaker output
- Channel mode for 5.1 speaker output
- Synchronize the phonejack switch with speakers settings

Select a speaker configuration by selecting its check circle, and then click **OK** to apply the configuration change.

Connect your speakers to the corresponding phonejacks. It is recommended you write down your configuration, power off the system, and then complete the physical connections.

Select from the **Phonejack Switch** section if you want to re-define the phonejacks. Click the specific phonejack button for several times to change its input/output functionality.

D.10 Speaker Test

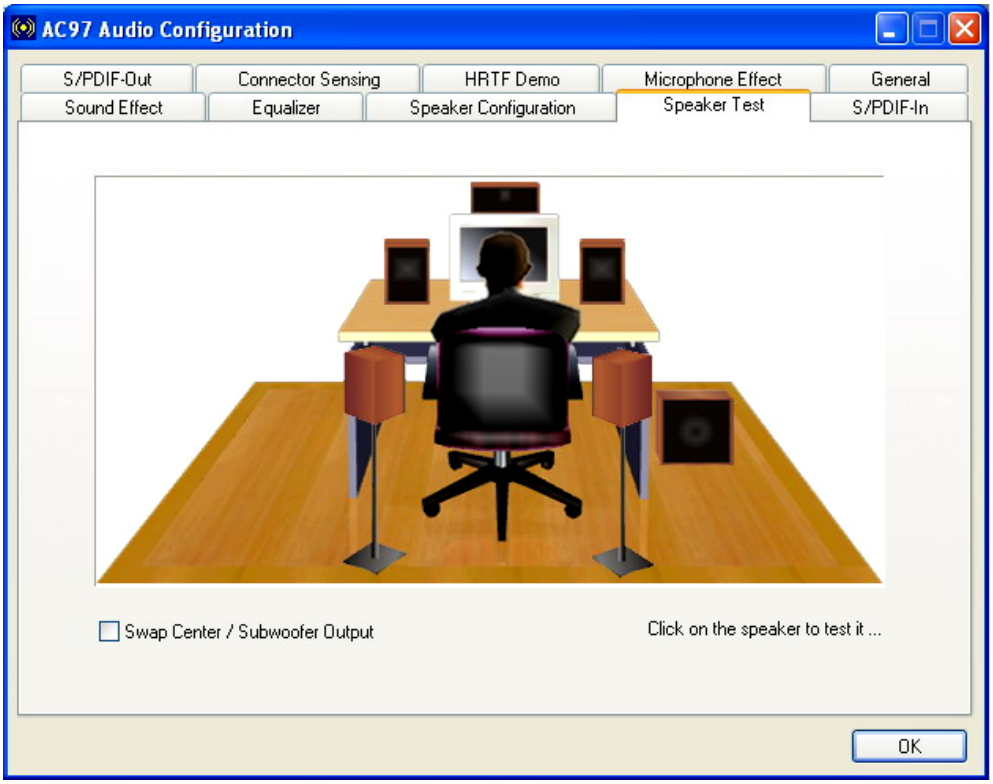

Figure D-11: Audio Configuration

The audio configuration window in **Figure D-11** allows you to test each connected speaker to see if your 4-channel or 6-channel audio operates properly. If any speaker malfunctions, you should then check the cabling or replace the malfunctioning parts.

Select each specific speaker to test its functionality. The speaker you select will be highlighted and sound should be generated.

NOTE:

1. The test scenario that appears in the **Speaker Test** window corresponds to the number of speakers you selected in the **Sound Effect** window.
2. You should select and deselect the **Swap Center/Subwoofer Output** check box to see if these two devices properly work.

D.11 S/PDIF-In & S/PDIF-Out

These functions are currently not supported.

D.12 Connector Sensing

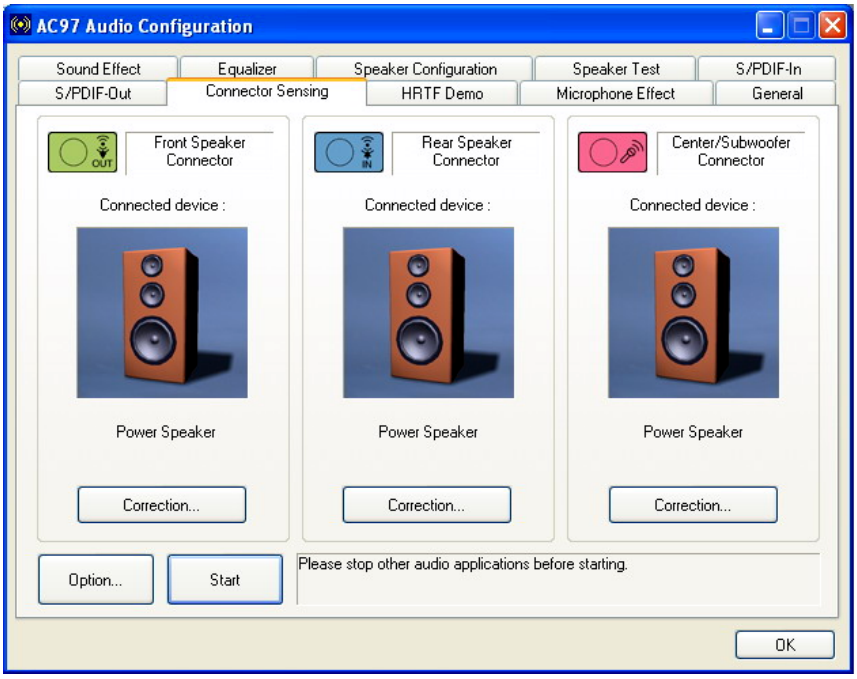

Figure D-12: Connector Sensing

Realtek ALC655 supports Jack Sensing functionality. If an audio device is plugged into the wrong connector, a warning message will display informing users to correct the physical connections.

Click the Start button in **Figure D-12** to start the sensing. Please remember to close all running audio-related programs before executing the sensing operation.

The EZ-Connection screen in **Figure D-13** shows the result of sensing test.

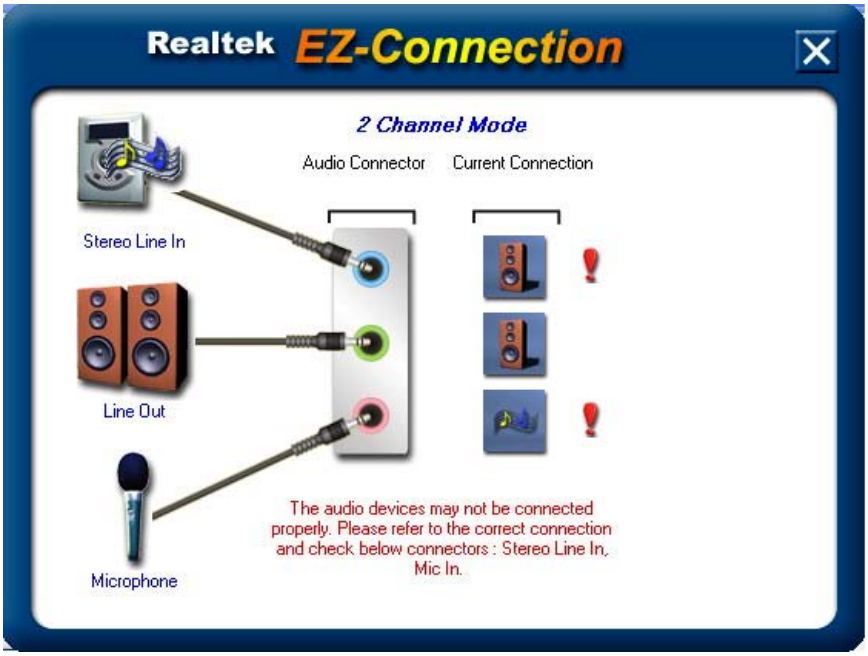

Figure D-13: EX Connection

The “Audio Connector” column shows the settings used in the “Speaker Configuration” window.

The “Current Connection” column shows the types of devices detected during test. If the result does not match the physical connection, an exclamation mark will appear. (See **Figure D-14**)

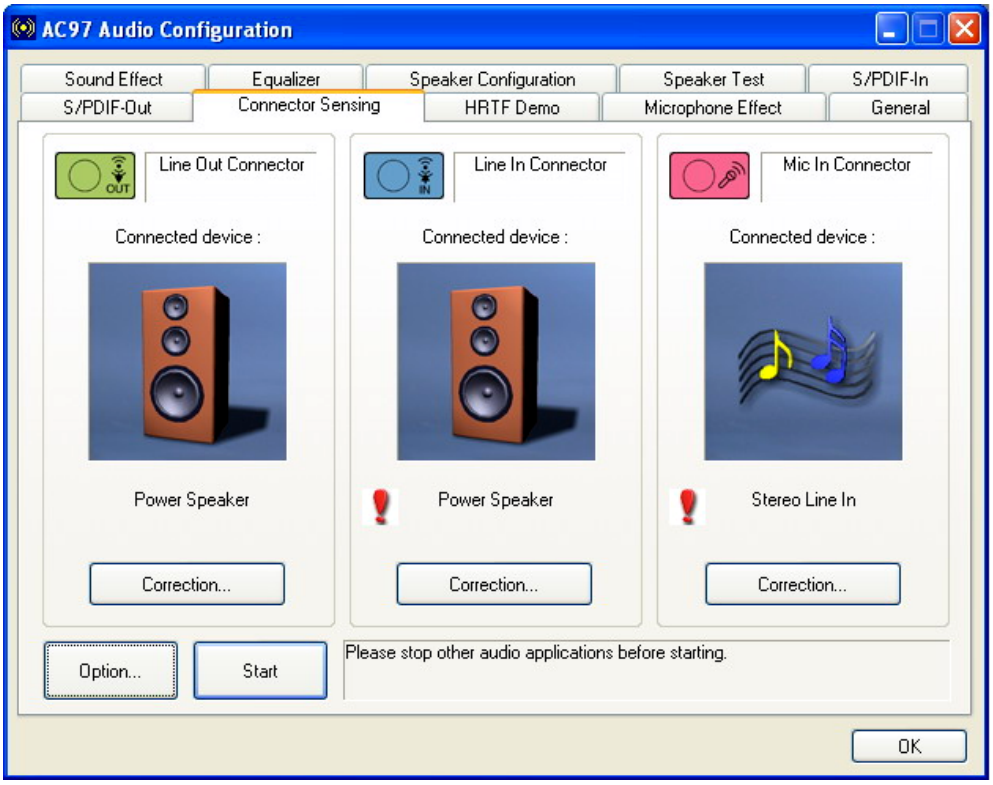

Figure D-14: Connector Sensing Test Result

After closing the EZ-Connector screen, the following window should appear showing the latest connection status.

D.13 HRTF Demo

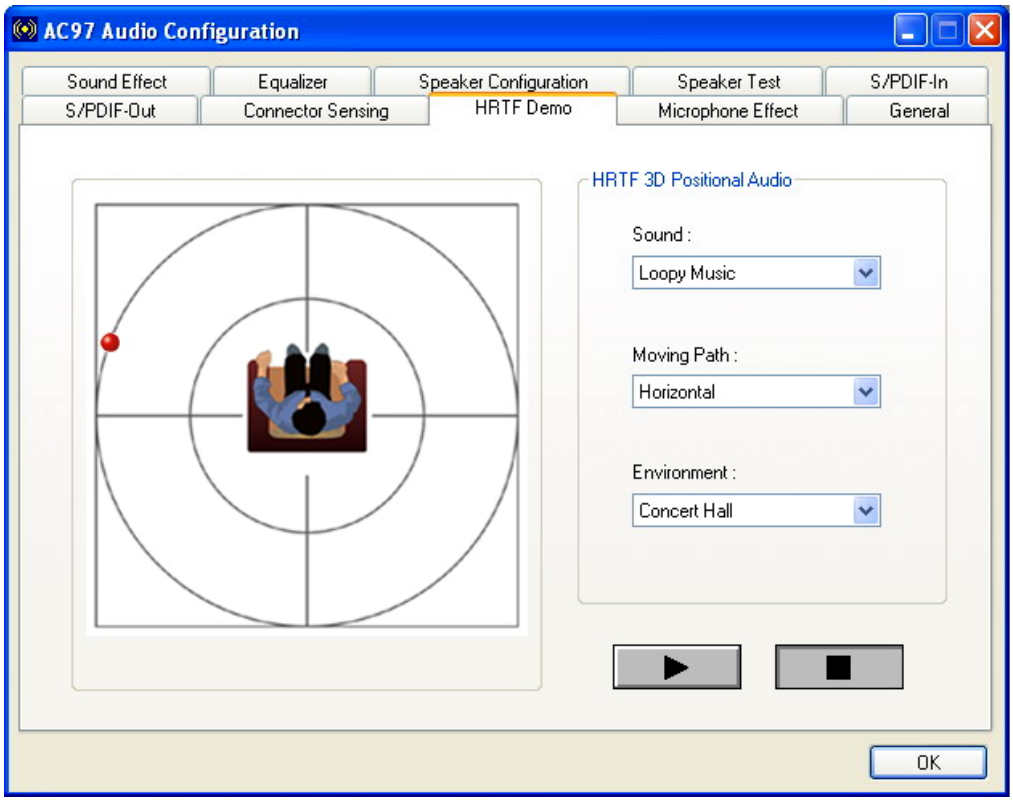

Figure D-15: HRTF Demo

The HRTF window in **Figure D-15** allows you to adjust your HRTF (Head Related Transfer Functions) 3D positional audio before playing 3D applications. Select a preferred **Environment** mode and/or different **Sound** and **Moving Path** settings.

D.14 Microphone Effect

This window provides a Noise Suppression option. Select its check box to enable this functionality.

D.15 General

The general window in **Figure D-16** provides information about this AC'97 audio configuration utility including **Audio Driver** version, **DirectX** version, **Audio Controller**, and **AC'97 Codec**. You may also change the language of this utility through the **Language** pull-down menu.

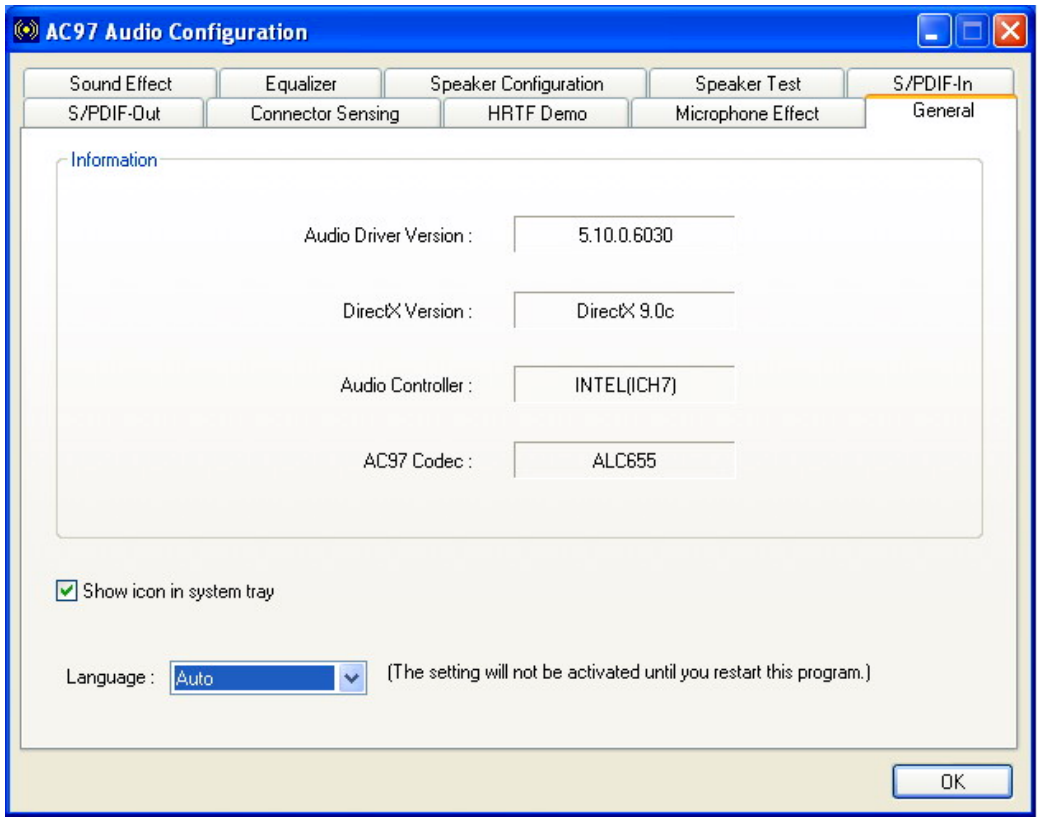

Figure D-16: General

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Product Service

Diagnosis and Debug

CyberResearch, Inc. maintains technical support lines staffed by experienced Applications Engineers and Technicians. There is no charge to call and we will return your call promptly if it is received while our lines are busy. Most problems encountered with data acquisition products can be solved over the phone. Signal connections and programming are the two most common sources of difficulty. CyberResearch support personnel can help you solve these problems, especially if you are prepared for the call.

To ensure your call's overall success and expediency:

1) Have the phone close to the PC so you can conveniently and quickly take action that the Applications Engineer might suggest.
2) Be prepared to open your PC, remove boards, report back-switch or jumper settings, and possibly change settings before reinstalling the modules.
3) Have a volt meter handy to take measurements of the signals you are trying to measure as well as the signals on the board, module, or power supply.
4) Isolate problem areas that are not working as you expected.
5) Have the source code to the program you are having trouble with available so that preceding and prerequisite modes can be referenced and discussed.
6) Have the manual at hand. Also have the product's utility disks and any other relevant disks nearby so programs and version numbers can be checked.

Preparation will facilitate the diagnosis procedure, save you time, and avoid repeated calls. Here are a few preliminary actions you can take before you call which may solve some of the more common problems:

1) Check the PC-bus power and any power supply signals.
2) Check the voltage level of the signal between SIGNAL HIGH and SIGNAL LOW, or SIGNAL+ and SIGNAL– . It CANNOT exceed the full scale range of the board.
3) Check the other boards in your PC or modules on the network for address and interrupt conflicts.
4) Refer to the example programs as a baseline for comparing code.

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Warranty Notice

CyberResearch, Inc. warrants that this equipment as furnished will be free from defects in material and workmanship for a period of one year from the confirmed date of purchase by the original buyer and that upon written notice of any such defect, CyberResearch, Inc. will, at its option, repair or replace the defective item under the terms of this warranty, subject to the provisions and specific exclusions listed herein.

This warranty shall not apply to equipment that has been previously repaired or altered outside our plant in any way which may, in the judgment of the manufacturer, affect its reliability. Nor will it apply if the equipment has been used in a manner exceeding or inconsistent with its specifications or if the serial number has been removed.

CyberResearch, Inc. does not assume any liability for consequential damages as a result from our products uses, and in any event our liability shall not exceed the original selling price of the equipment.

The equipment warranty shall constitute the sole and exclusive remedy of any Buyer of Seller equipment and the sole and exclusive liability of the Seller, its successors or assigns, in connection with equipment purchased and in lieu of all other warranties expressed implied or statutory, including, but not limited to, any implied warranty of merchant ability or fitness and all other obligations or liabilities of seller, its successors or assigns.

The equipment must be returned postage prepaid. Package it securely and insure it. You will be charged for parts and labor if the warranty period has expired.

Returns and RMAs

If a CyberResearch product has been diagnosed as being non-functional, is visibly damaged, or must be returned for any other reason, please call for an assigned RMA number. The RMA number is a key piece of information that lets us track and process returned merchandise with the fastest possible turnaround time.

PLEASE CALL FOR AN RMA NUMBER!

Packages returned without an RMA number will be refused!

In most cases, a returned package will be refused at the receiving dock if its contents are not known. The RMA number allows us to reference the history of returned products and determine if they are meeting your application's requirements. When you call customer service for your RMA number, you will be asked to provide information about the product you are returning, your address, and a contact person at your organization.

Please make sure that the RMA number is prominently displayed on the outside of the box.

• Thank You •

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